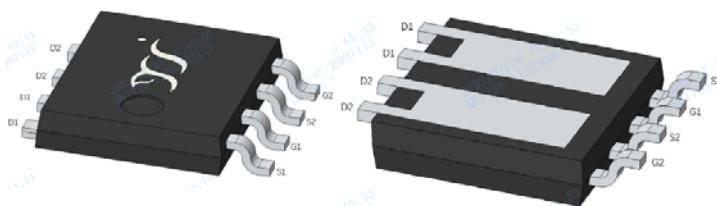
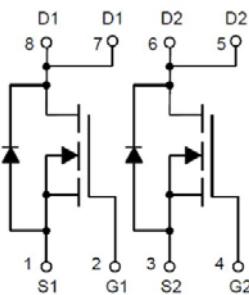


N-Channel Enhancement Mode Field Effect Transistor

**LFPAK56D**

Product Summary

- V_{DS} 40V
- I_D 69A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) $<5.8m\Omega$
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free
- Part no. with suffix "Q" means AEC-Q101 qualified

Applications

- 12V Automotive systems
- Motors, lamps and solenoid control

Absolute Maximum Ratings ($T_J=25^\circ C$ unless otherwise noted)

Parameter			Symbol	Limit	Unit
Drain-source Voltage			V_{DS}	40	V
Gate-source Voltage			V_{GS}	± 20	V
Continuous Drain Current (Note 1,2)	Steady-State	$T_A=25^\circ C, V_{GS}= 10V$	I_D	14	A
		$T_A=100^\circ C, V_{GS}= 10V$		10	
Continuous Drain Current (Note 1,3)	Steady-State	$T_c=25^\circ C, V_{GS}= 10V$	I_D	69	A
		$T_c=100^\circ C, V_{GS}= 10V$		48	
Pulsed Drain Current	$T_c=25^\circ C, t_p=100\mu s$		I_{DM}	270	A
Avalanche energy	$V_G=10V, R_G=25\Omega, L=0.5mH, IAS=16A$		EAS	64	mJ
Total Power Dissipation (Note 1,2)	Steady-State	$T_A=25^\circ C$	P_D	3	W
		$T_A=100^\circ C$		1.5	
Total Power Dissipation (Note 1,3)	Steady-State	$T_c=25^\circ C$	P_D	65	
		$T_c=100^\circ C$		32	
Junction and Storage Temperature Range			T_J, T_{STG}	-55~+175	°C

Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	40	50	°C/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	1.8	2.3	

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJYAD5D8G04HRHQ	F1	YAD5D8G04HR	5000	10000	100000	13" reel



YJYAD5D8G04HRHQ

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	40	-		V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V, V _{GS} =0V	-	-	1	μA
		V _{DS} =40V, V _{GS} =0V, T _J =125°C	-		100	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2.0	2.9	4.0	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	5	5.8	mΩ
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V	-	-	1.2	V
Gate resistance	R _G	f=1MHz	-	2.5	-	Ω
Maximum Body-Diode Continuous Current	I _S		-	-	69	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1MHz	-	1017	-	pF
Output Capacitance	C _{oss}		-	300	-	
Reverse Transfer Capacitance	C _{rss}		-	10.3	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =20V, I _D =30A	-	13.5	-	nC
Gate-Source Charge	Q _{gs}		-	4.8	-	
Gate-Drain Charge	Q _{gd}		-	2.9	-	
Reverse Recovery Charge	Q _{rr}	I _F =30A, di/dt=100A/us	-	94	-	nC
Reverse Recovery Time	t _{rr}		-	68.4	-	ns
Turn-on Delay Time	t _{D(on)}		-	8.6	-	ns
Turn-on Rise Time	t _r	V _{GS} =10V, V _{DD} =20V, I _D =30A R _{GEN} =2.5Ω	-	104.7	-	
Turn-off Delay Time	t _{D(off)}		-	11.56	-	
Turn-off fall Time	t _f		-	10.5	-	

Note:

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- The value of R_{θJA} is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with TA =25°C. The maximum allowed junction temperature of 175°C. The value in any given application depends on the user's specific board design.
- Thermal resistance from junction to soldering point (on the exposed drain pad).

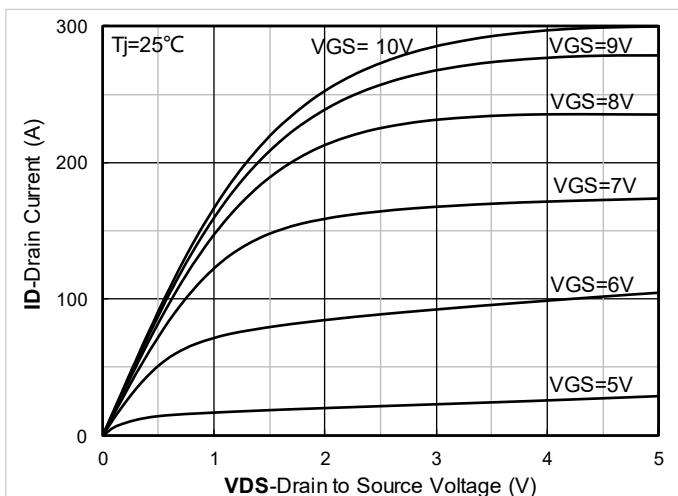
**■Typical Electrical and Thermal Characteristics Diagrams**

Figure 1. Output Characteristics

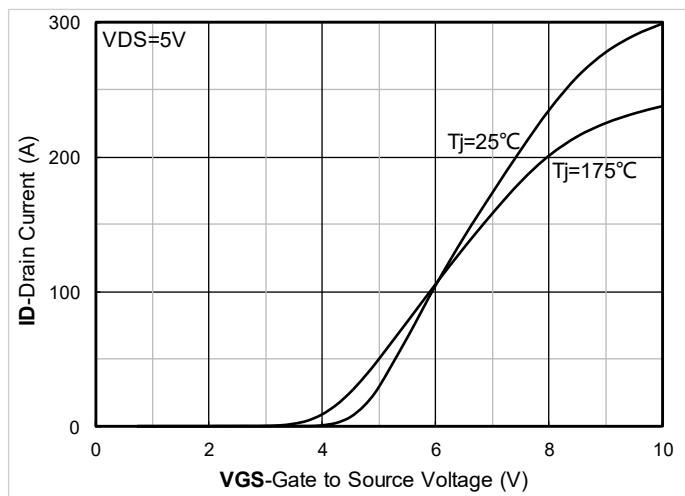


Figure 2. Transfer Characteristics

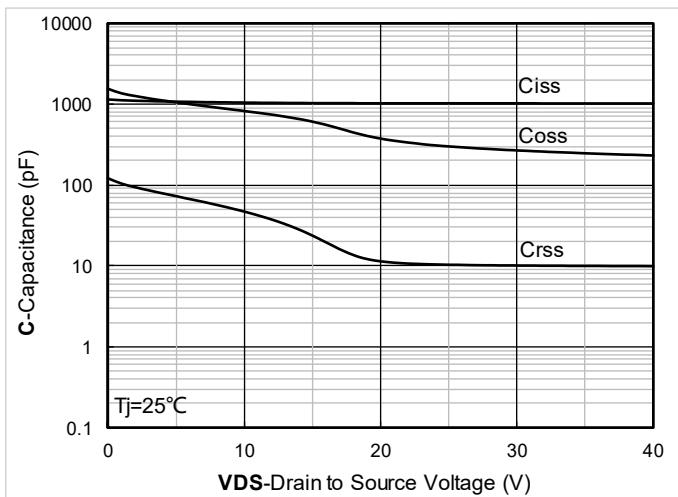


Figure 3. Capacitance Characteristics

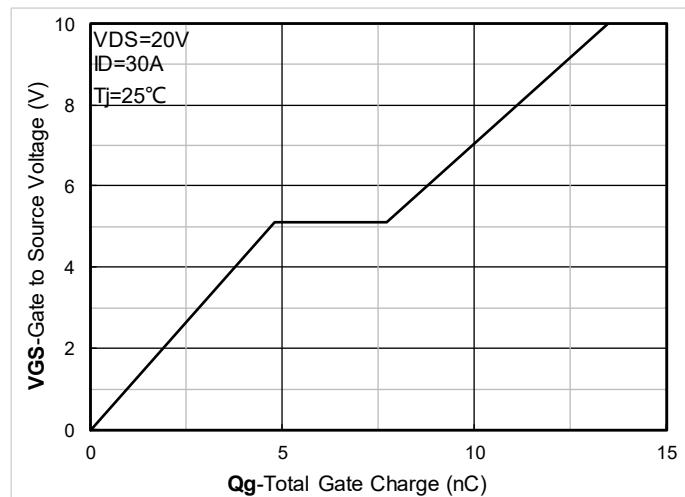


Figure 4. Gate Charge

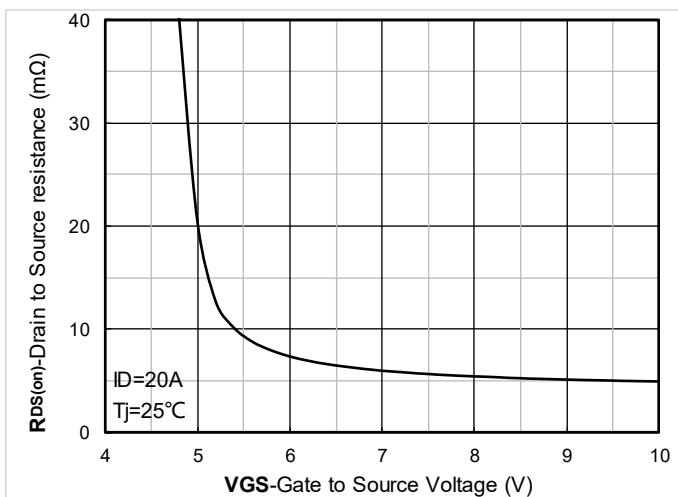


Figure 5. On-Resistance vs Gate to Source Voltage

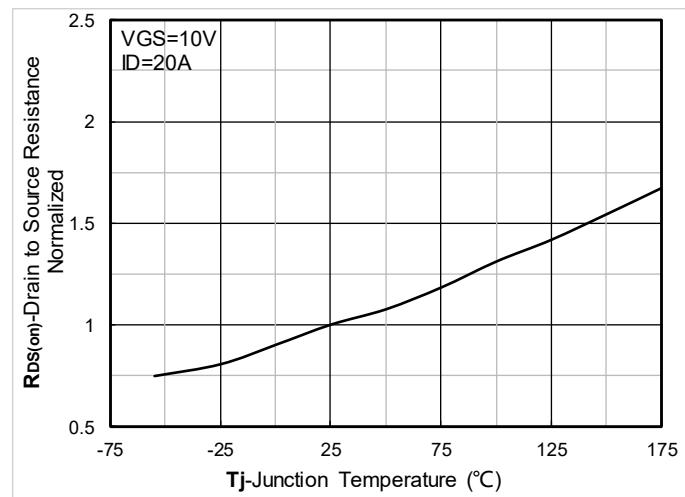


Figure 6. Normalized On-Resistance

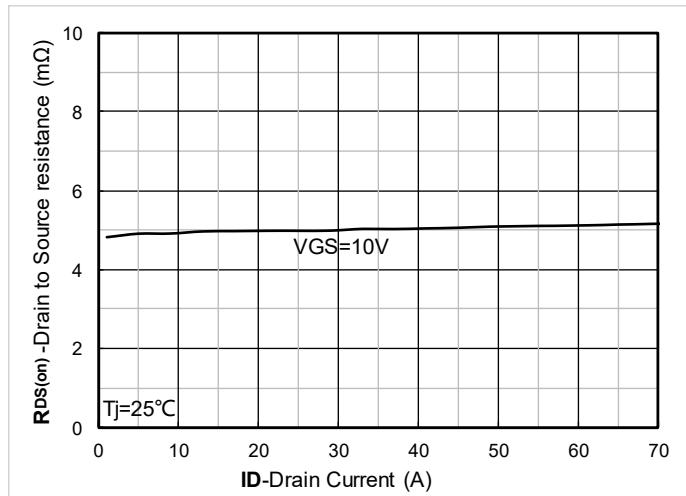


Figure 7. RDS(on) VS Drain Current

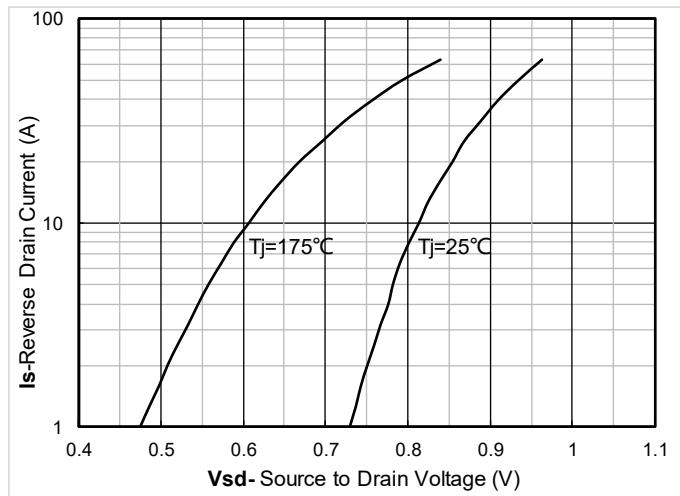


Figure 8. Forward characteristics of reverse diode

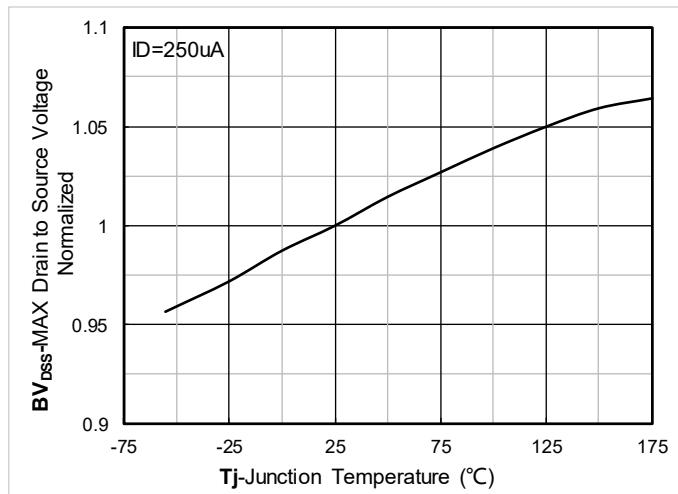


Figure 9. Normalized breakdown voltage

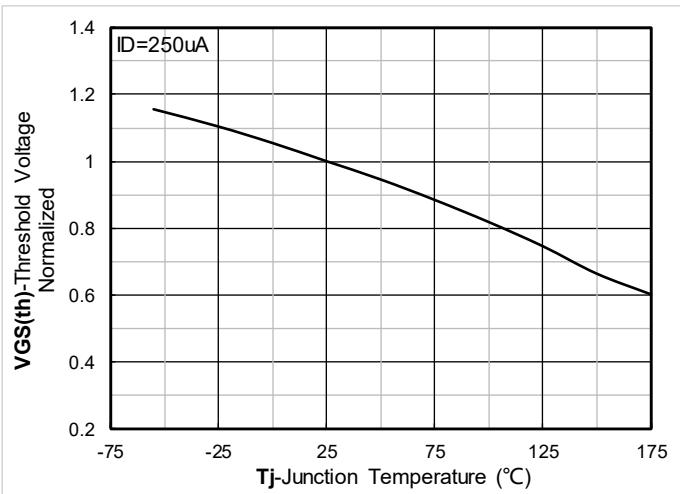


Figure 10. Normalized Threshold voltage

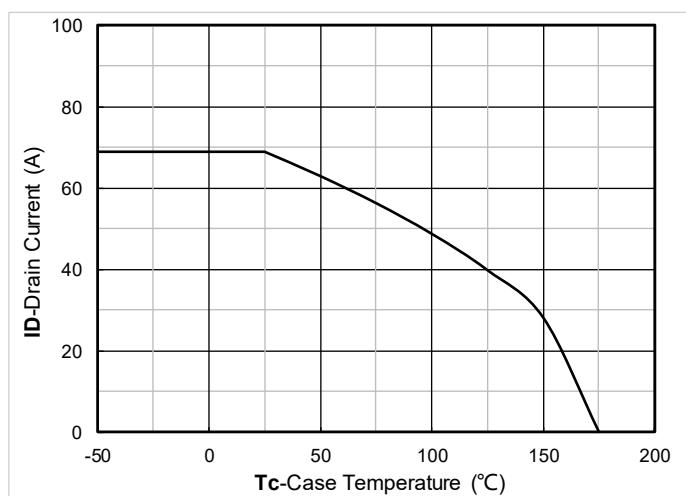


Figure 11. Current dissipation

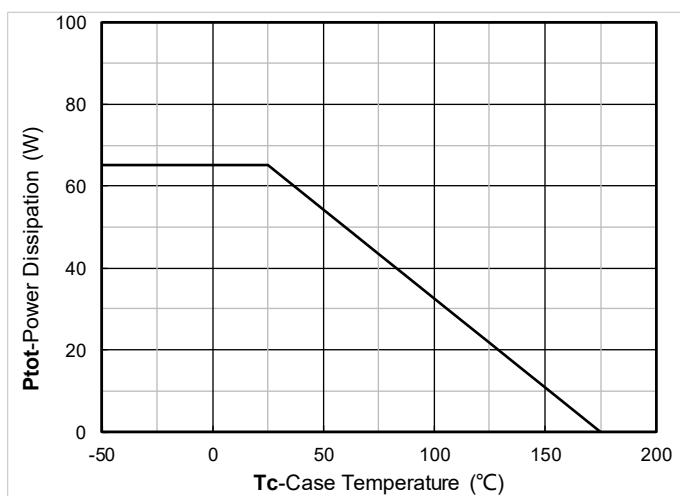


Figure 12. Power dissipation



YJYAD5D8G04HRHQ

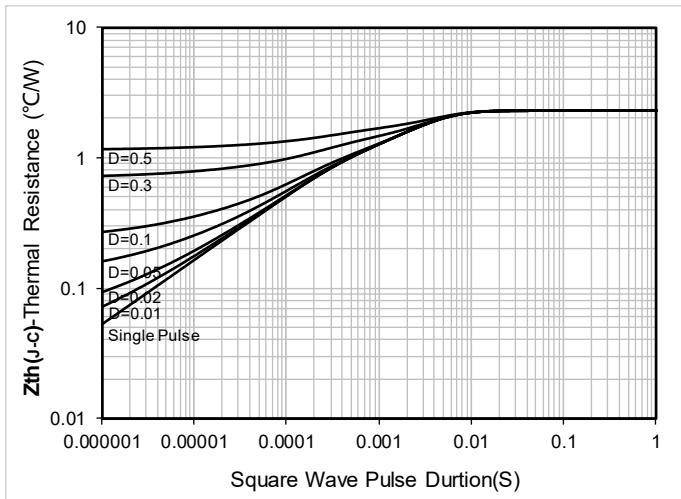


Figure 13. Maximum Transient Thermal Impedance

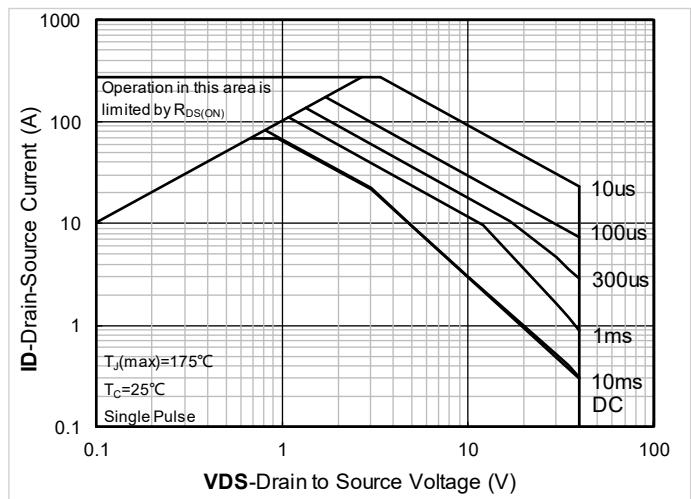
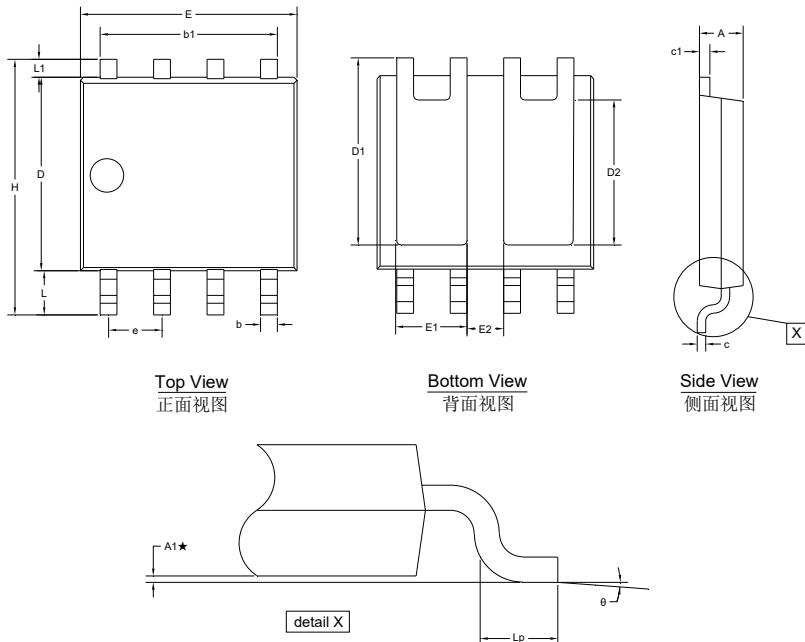


Figure 14. Safe Operation Area



■ LFPAK56D Package information



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.10\text{mm}$.
3. The pad layout is for reference purposes only.
4. ★ It is the key size.

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.0200	1.0400	1.0500
A1★	0.00	0.0500	0.10
b	0.3500		0.5500
b1	4.10	4.2500	4.40
c	0.1900	0.2200	0.2500
c1	0.2400	0.2700	0.30
D	4.4500	4.6000	4.70
D1	4.3500	4.4500	4.5500
D2	3.40	3.4500	3.50
E	4.9500	5.1500	5.30
E1	1.60	1.7000	1.80
E2	0.77	0.8700	0.97
e		1.2700	
H	5.90		6.20
L	0.80	1.0500	1.30
L1	0.30	0.4250	0.55
Lp	0.40	0.6250	0.85
θ	0°		8°



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