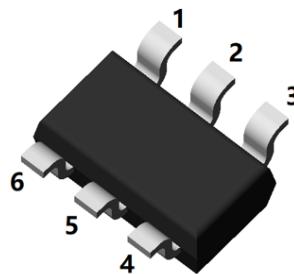
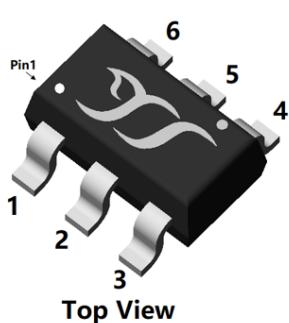
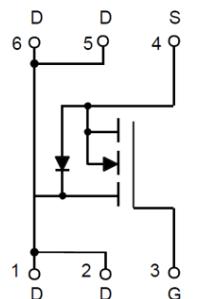


**N-Channel Enhancement Mode Field Effect Transistor****SOT-23-6L****Product Summary**

- V_{DS} 100V
- I_D 3.0A
- $R_{DS(ON)}$ (at $V_{GS} = 10V$) <120mohm
- $R_{DS(ON)}$ (at $V_{GS} = 4.5V$) <140mohm

General Description

- Trench Power MV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- DC-DC Converters
- Power management functions

■ Absolute Maximum Ratings (T_A=25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	T _A =25°C	I_D	3	A
	T _A =70°C		2.4	
Pulsed Drain Current ^A		I_{DM}	12	A
Single Pulse Avalanche Energy		E_{AS}	8	mJ
Total Power Dissipation @ T _A =25°C		P_D	1.5	W
Thermal Resistance Junction-to-Ambient ^B		$R_{\theta JA}$	83	°C/W
Thermal Resistance From Junction To Lead		$R_{\theta JL}$	36	°C/W
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	°C

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJS03N10A	F2	1003	3000	30000	120000	7"



YJS03N10A

■ Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	100			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}}=100\text{V}, V_{\text{GS}}=0\text{V}$			1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{\text{GS}}= \pm 20\text{V}, V_{\text{DS}}=0\text{V}$			± 100	nA
Gate Threshold Voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	1.1	1.8	3.0	V
Static Drain-Source On-Resistance	$R_{\text{DS(ON)}}$	$V_{\text{GS}}= 10\text{V}, I_{\text{D}}=3\text{A}$		95	120	$\text{m}\Omega$
		$V_{\text{GS}}= 4.5\text{V}, I_{\text{D}}=2.4\text{A}$		100	140	
Diode Forward Voltage	V_{SD}	$I_{\text{S}}=3\text{A}, V_{\text{GS}}=0\text{V}$		0.8	1.2	V
Maximum Body-Diode Continuous Current	I_{S}				3	A
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{\text{DS}}=50\text{V}, V_{\text{GS}}=0\text{V}, f=1\text{MHz}$		1070		pF
Output Capacitance	C_{oss}			33		
Reverse Transfer Capacitance	C_{rss}			30		
Switching Parameters						
Total Gate Charge	Q_{g}	$V_{\text{GS}}=10\text{V}, V_{\text{DS}}=50\text{V}, I_{\text{D}}=10\text{A}$		26		nC
Gate-Source Charge	Q_{gs}			5.4		
Gate-Drain Charge	Q_{gd}			5.8		
Reverse Recovery Charge	Q_{rr}	$I_{\text{F}}=10\text{A}, \text{di}/\text{dt}=100\text{A}/\text{us}$		30.1		ns
Reverse Recovery Time	t_{rr}			40		
Turn-on Delay Time	$t_{\text{D(on)}}$	$V_{\text{GS}}=10\text{V}, V_{\text{DD}}=50\text{V}, R_{\text{L}}=6.4\Omega, R_{\text{GEN}}=3\Omega$		7		ns
Turn-on Rise Time	t_{r}			24		
Turn-off Delay Time	$t_{\text{D(off)}}$			24		
Turn-off fall Time	t_{f}			31		

A. Pulse Test: Pulse Width $\leq 300\text{us}$, Duty cycle $\leq 2\%$.

B. R_{\thetaJA} is the sum of the junction-to-lead and lead-to-ambient thermal resistance, where the lead thermal reference is defined as the solder mounting surface of the drain pins. R_{\thetaJL} is guaranteed by design, while R_{\thetaJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ Typical Performance Characteristics

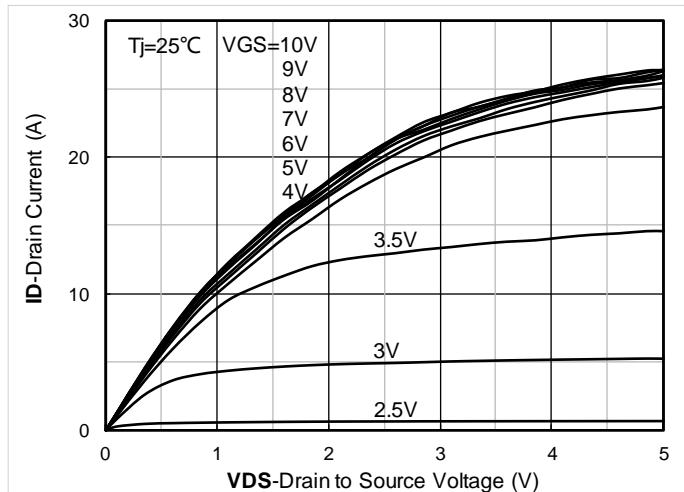


Figure 1. Output Characteristics

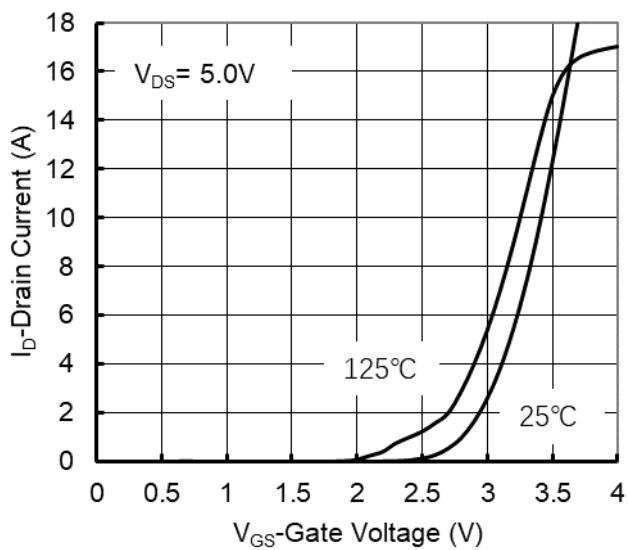


Figure 2. Transfer Characteristics

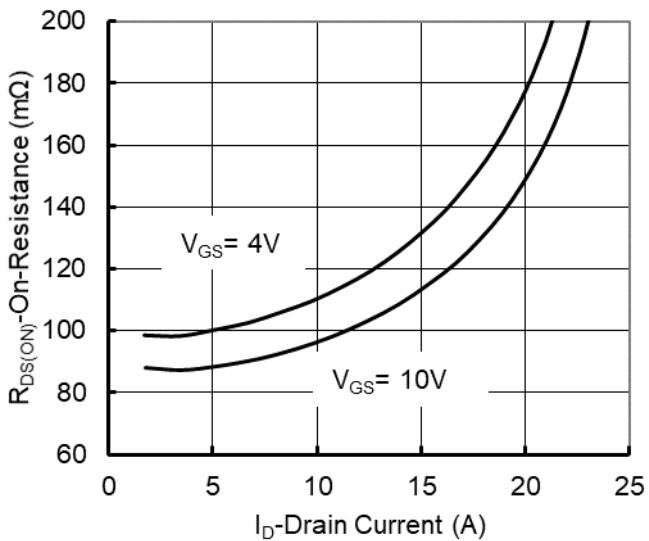


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

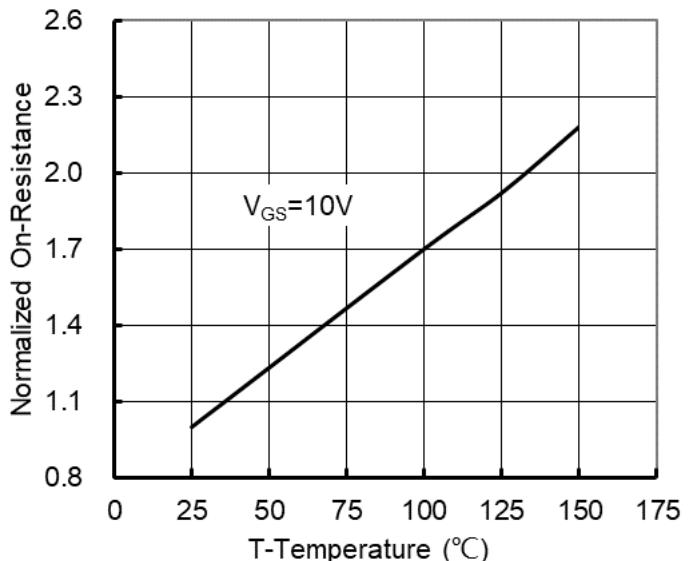


Figure 4. On-Resistance vs. Junction Temperature

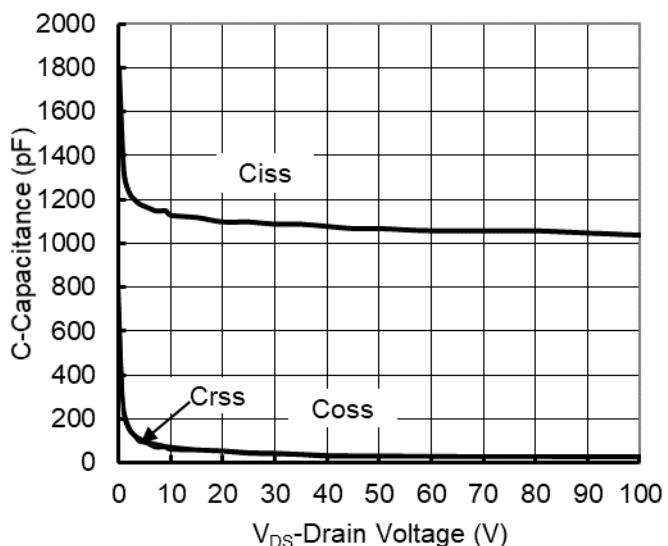


Figure 5. Capacitance Characteristics

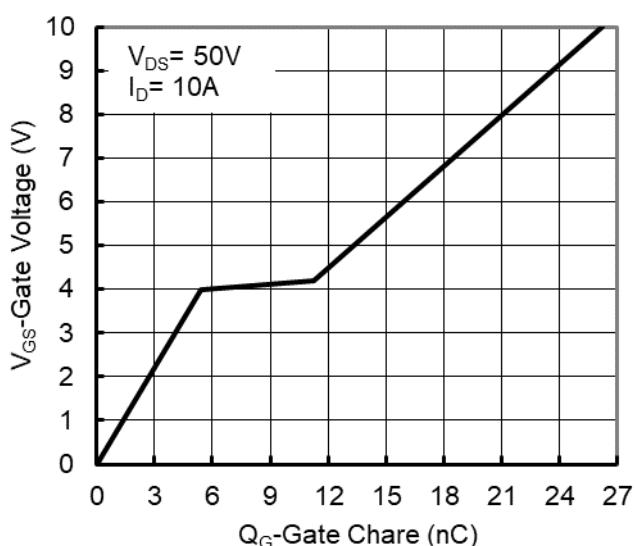


Figure 6. Gate Charge

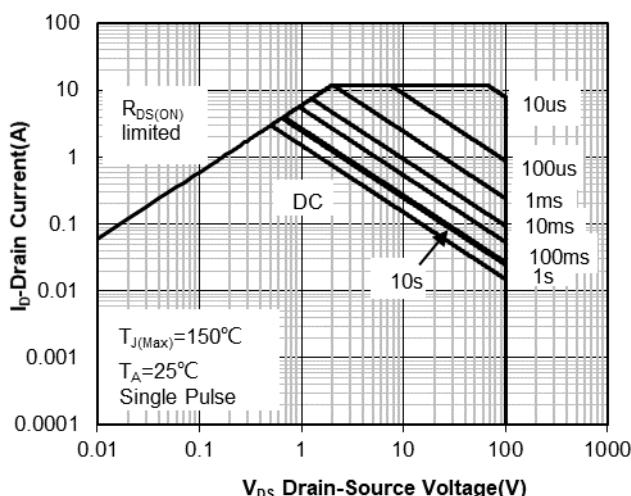


Figure 7. Safe Operation Area

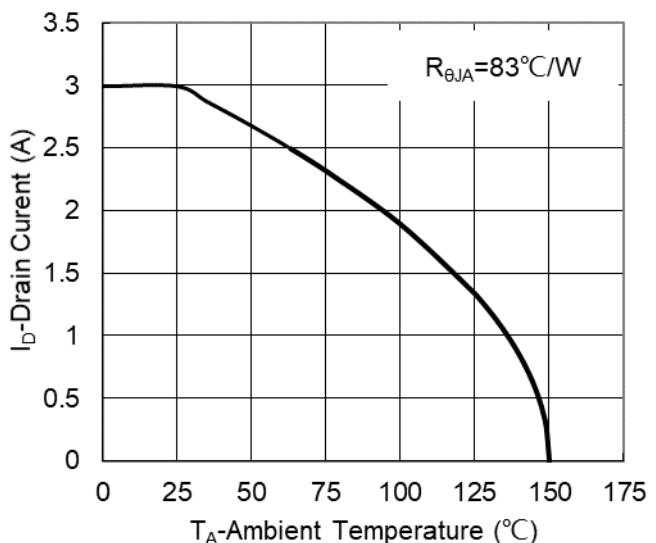


Figure 8. Maximum Continuous Drain Current vs Ambient Temperature

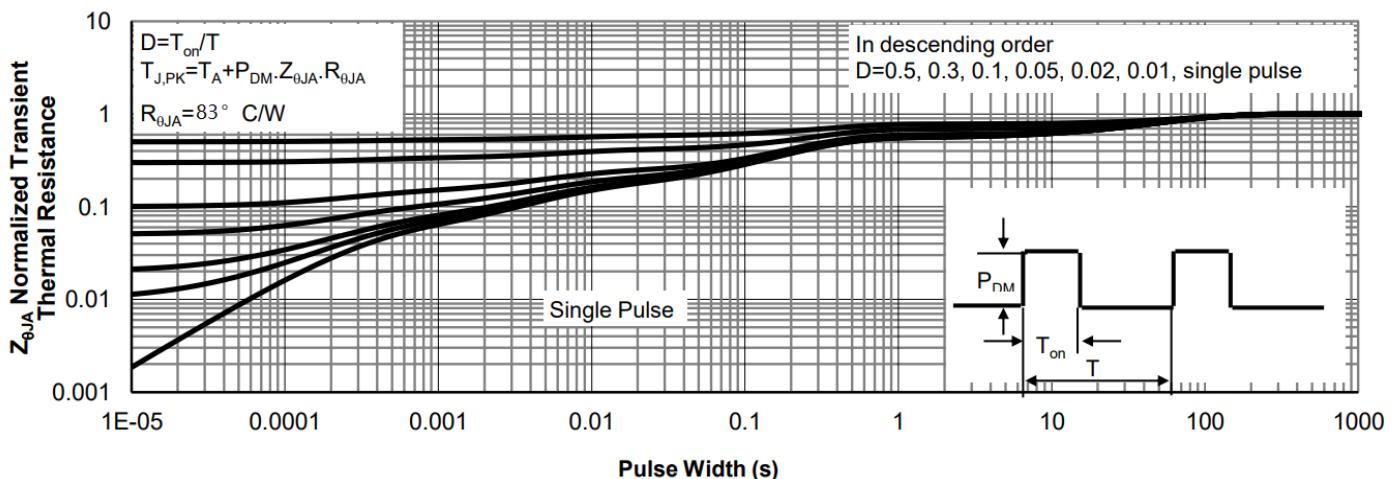


Figure 9. Normalized Maximum Transient Thermal Impedance

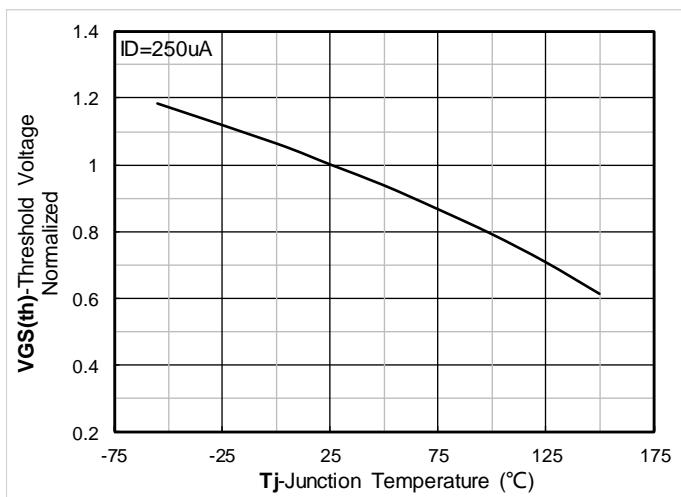
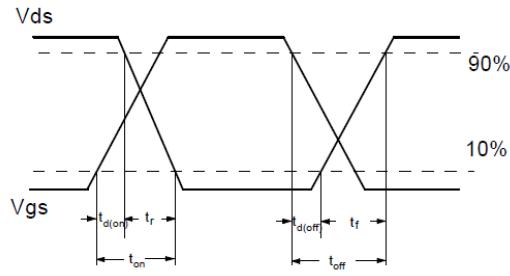
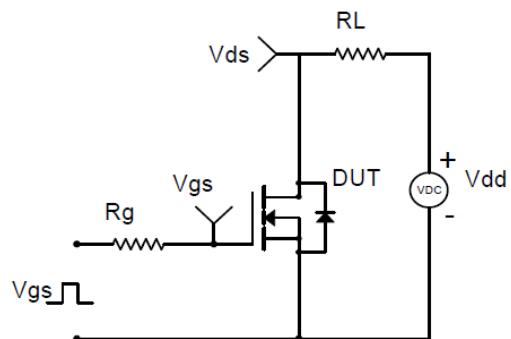
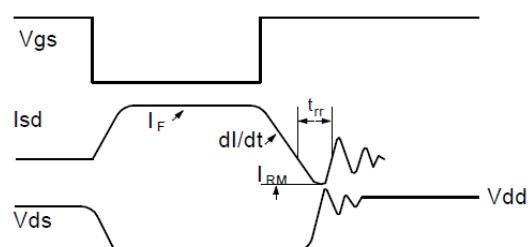
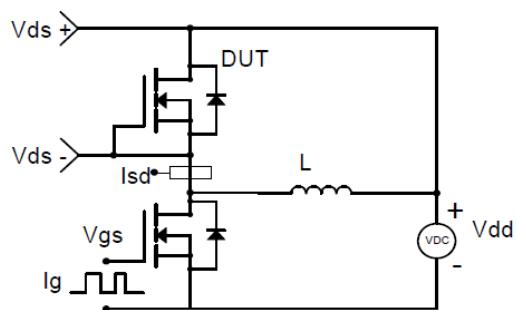


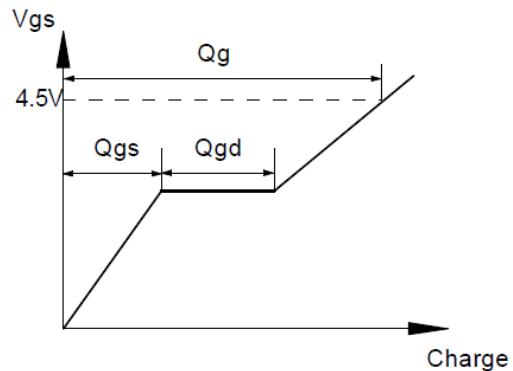
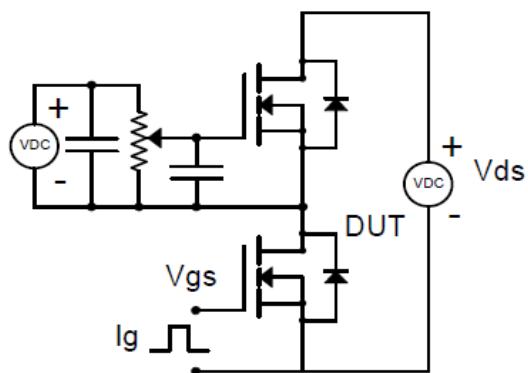
Figure 10. Normalized Threshold voltage



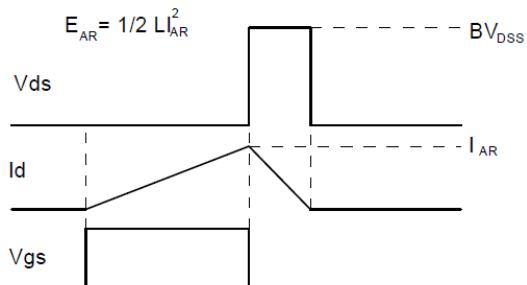
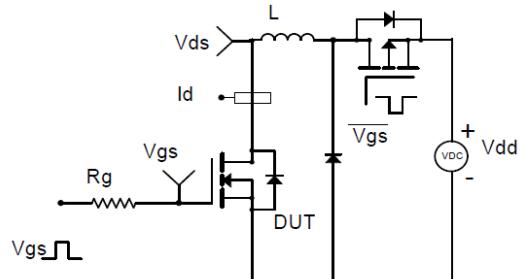
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



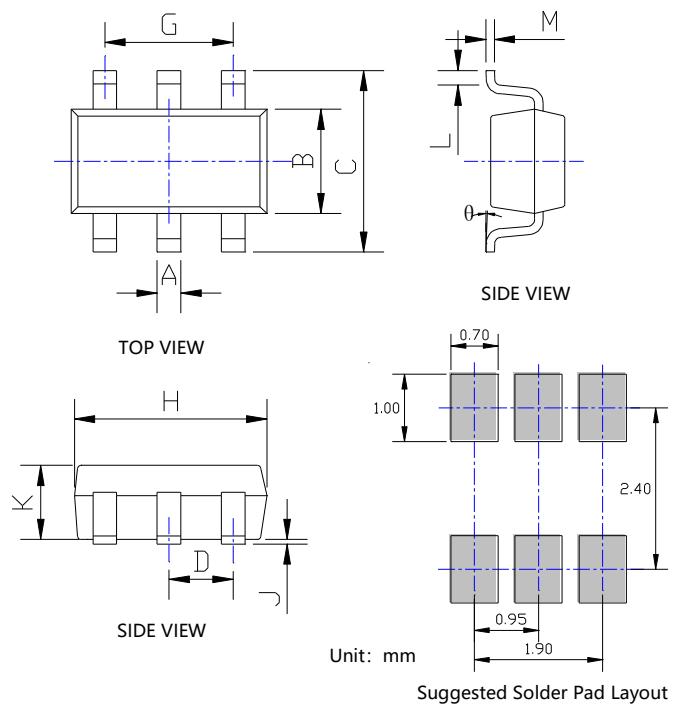
Gate Charge Test Circuit & Waveform



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



■SOT-23-6L Package information



SYMBOL	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.012	0.020	0.300	0.500
B	0.059	0.067	1.500	1.700
C	0.104	0.116	2.650	2.950
D	0.037BSC		0.950BSC	
G	0.075BSC		1.900BSC	
H	0.111	0.119	2.820	3.020
J	0.000	0.004	0.000	0.100
K	0.041	0.045	1.050	1.150
L	0.012	0.024	0.300	0.600
M	0.004	0.008	0.100	0.200
θ	0°	8°	0°	8°

Note:

1. Controlling dimension:in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.



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