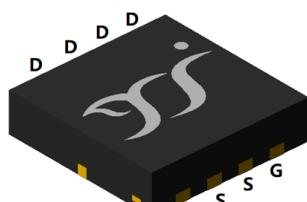
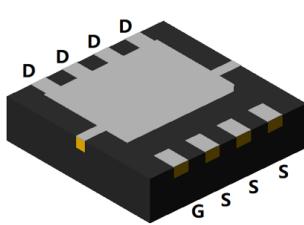


P-Channel Enhancement Mode Field Effect Transistor

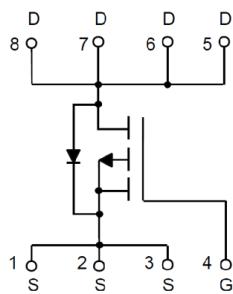


Top View



Bottom View

DFN3333-8L



Product Summary

- V_{DS} -20V
- I_D -55A
- $R_{DS(ON)}$ (at $V_{GS} = -4.5V$) < 8.3mohm
- $R_{DS(ON)}$ (at $V_{GS} = -2.5V$) < 10.0mohm
- $R_{DS(ON)}$ (at $V_{GS} = -1.8V$) < 15.0mohm
- 100% EAS Tested

General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- High current load applications
- Load switching
- Hard switched and high frequency Circuits
- Uninterruptible power supply

Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	-20	V
Gate-source Voltage		V_{GS}	± 10	V
Drain Current	$T_c=25^\circ C$	I_D	-55	A
	$T_c=100^\circ C$		-35	
Pulsed Drain Current ^A		I_{DM}	-160	A
Single Pulse Avalanche Energy ^B		E_{AS}	75	mJ
Total Power Dissipation	$T_c=25^\circ C$	P_D	38	W
	$T_c=100^\circ C$		15	
Thermal Resistance Junction-to-Case ^C		$R_{\theta JC}$	3.3	$^\circ C/W$
		$R_{\theta JA}$	39	
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ C$

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ55P02A	F1	Q55P02A	5000	10000	100000	13" reel

■ Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=-250\mu\text{A}$	-20			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}}=-20\text{V}, V_{\text{GS}}=0\text{V}$			-1	μA
		$V_{\text{DS}}=-20\text{V}, V_{\text{GS}}=0\text{V}, T_J=150^\circ\text{C}$			-100	
Gate-Body Leakage Current	I_{GSS}	$V_{\text{GS}}= \pm 10\text{V}, V_{\text{DS}}=0\text{V}$			± 100	nA
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}}= V_{\text{GS}}, I_{\text{D}}=-250\mu\text{A}$	-0.4	-0.62	-1.0	V
Static Drain-Source On-Resistance	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}}= -4.5\text{V}, I_{\text{D}}=-15\text{A}$		6.5	8.3	$\text{m}\Omega$
		$V_{\text{GS}}= -2.5\text{V}, I_{\text{D}}=-10\text{A}$		8.0	10.0	
		$V_{\text{GS}}= -1.8\text{V}, I_{\text{D}}=-8.0\text{A}$		10.3	15.0	
Diode Forward Voltage	V_{SD}	$I_{\text{S}}=20\text{A}, V_{\text{GS}}=0\text{V}$		-0.7	-1.2	V
Maximum Body-Diode Continuous Current	I_{S}				-55	A
Gate resistance	R_g	F=1 MHz, Open drain		7.1		Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{\text{DS}}=-10\text{V}, V_{\text{GS}}=0\text{V}, f=1\text{MHz}$		6358		pF
Output Capacitance	C_{oss}			690		
Reverse Transfer Capacitance	C_{rss}			477		
Switching Parameters						
Total Gate Charge	Q_g	$V_{\text{GS}}=-10\text{V}, V_{\text{DS}}=-15\text{V}, I_{\text{D}}=-9.1\text{A}$		149		nC
Gate-Source Charge	Q_{gs}			12.7		
Gate-Drain Charge	Q_{gd}			21		
Reverse Recovery Charge	Q_{rr}	$I_F=-6\text{A}, dI/dt=100\text{A/us}$		25.2		ns
Reverse Recovery Time	t_{rr}			46		
Turn-on Delay Time	$t_{\text{D(on)}}$			11		
Turn-on Rise Time	t_r	$V_{\text{GS}}=-10\text{V}, V_{\text{DD}}=-15\text{V}, I_{\text{D}}=-6\text{A}$ $R_{\text{GEN}}=2.5\Omega$		36		ns
Turn-off Delay Time	$t_{\text{D(off)}}$			182		
Turn-off fall Time	t_f			191		

A. Pulse Test: Pulse Width $\leqslant 300\text{us}$, Duty cycle $\leqslant 2\%$.B. $T_J=25^\circ\text{C}$, $V_{\text{DD}}=20\text{V}$, $V_G=10\text{V}$, $L=0.5\text{mH}$, $I_{\text{AS}}=17.4\text{A}$ C. The value of R_{GJA} is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design.

■ Typical Performance Characteristics

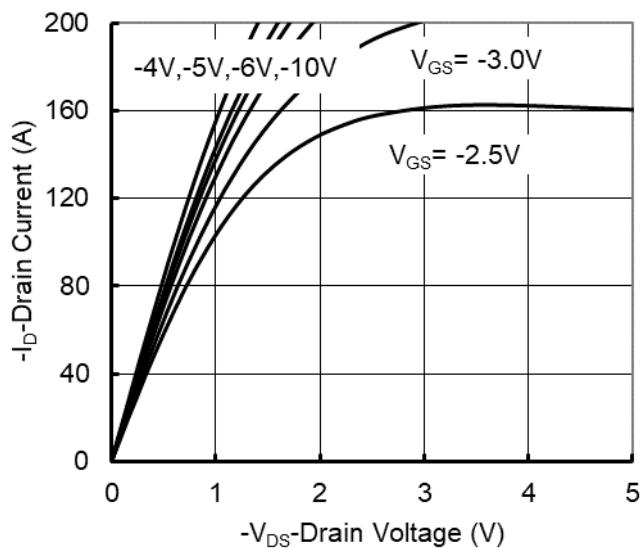


Figure 1. Output Characteristics

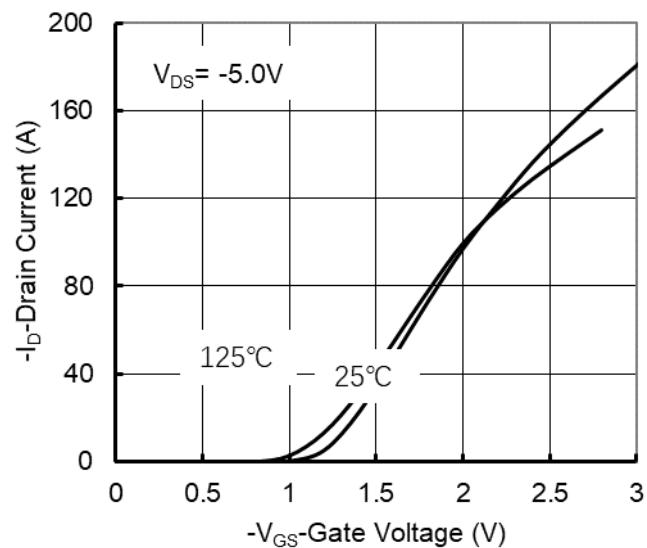


Figure 2. Transfer Characteristics

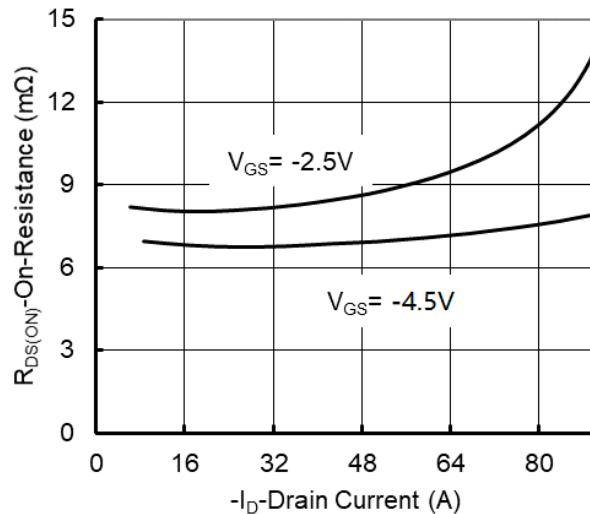


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

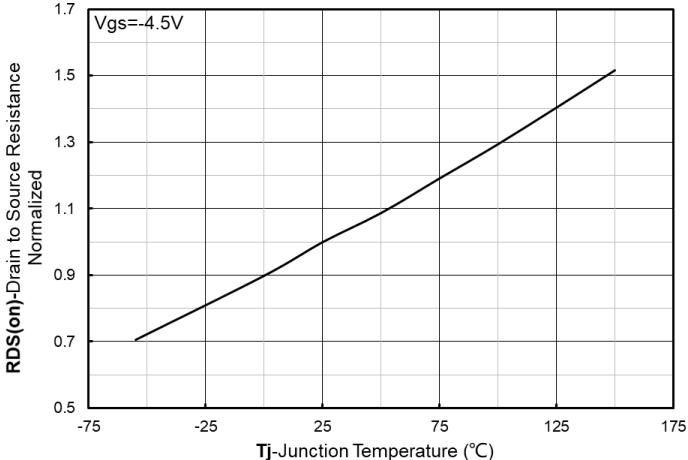


Figure 4. On-Resistance vs. Junction Temperature

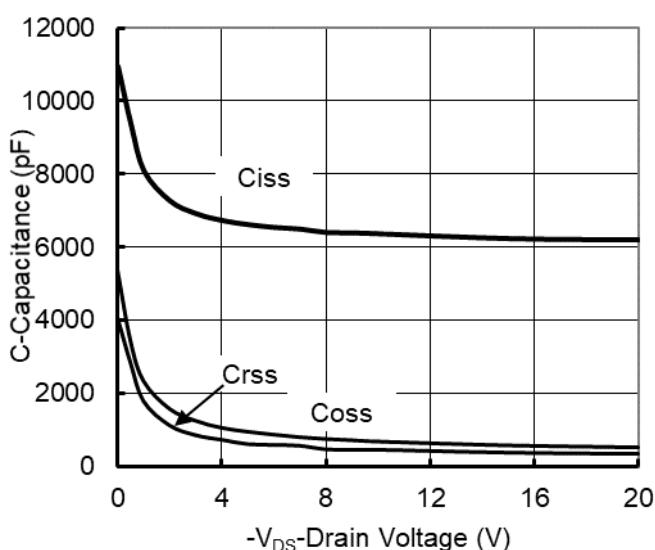


Figure 5. Capacitance Characteristics

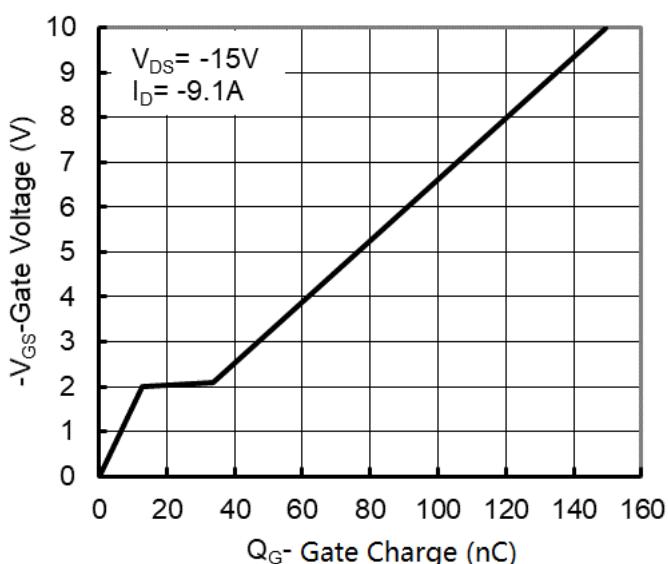
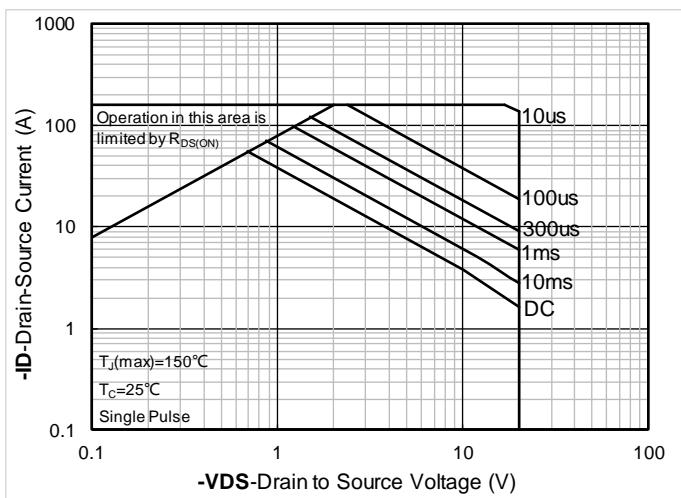
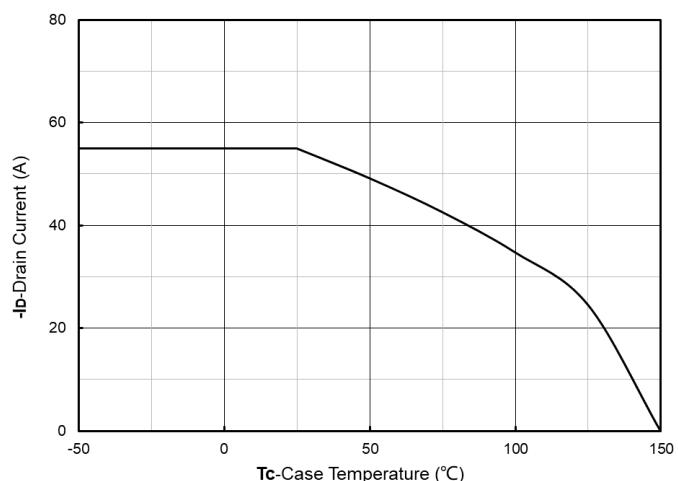
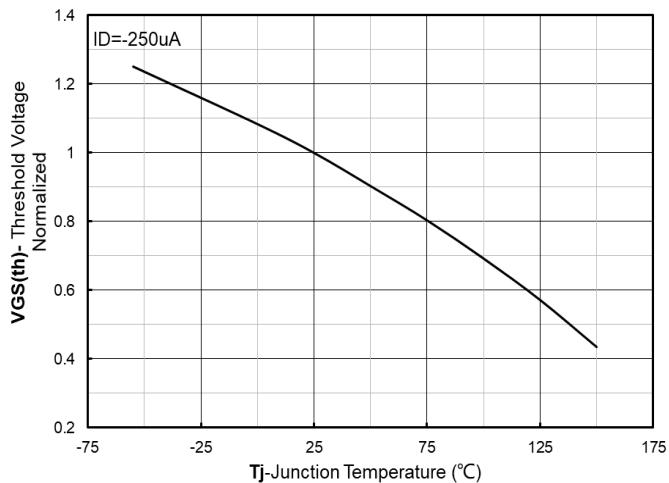
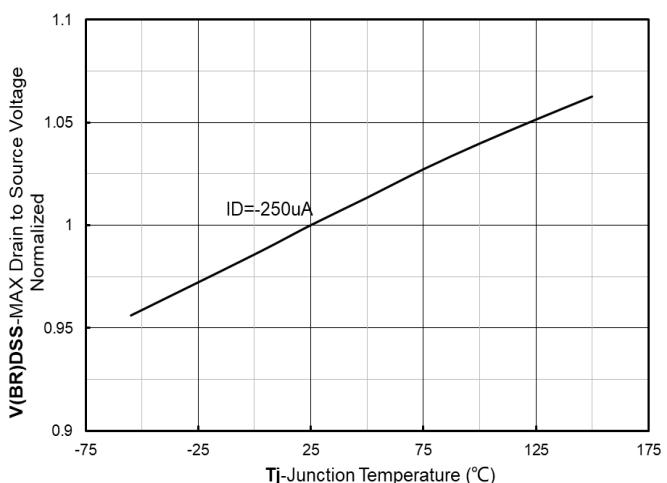
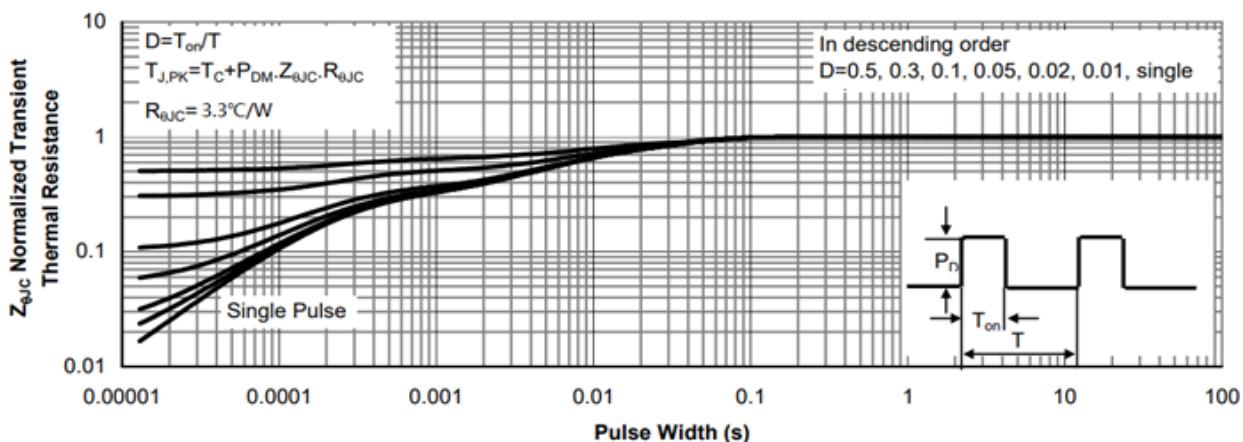
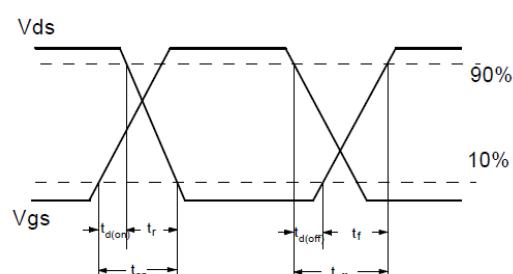
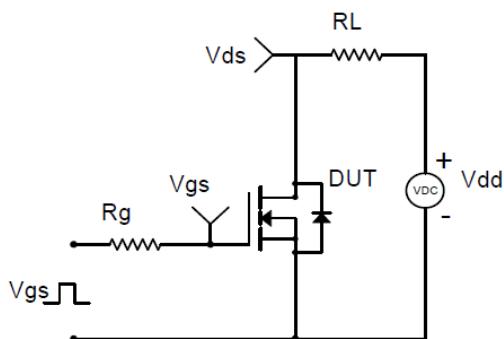
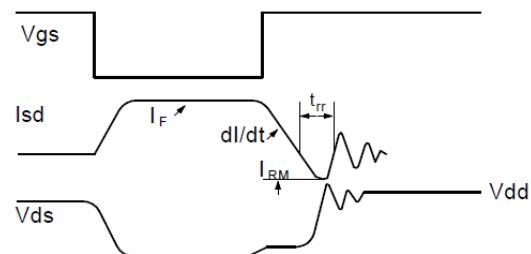
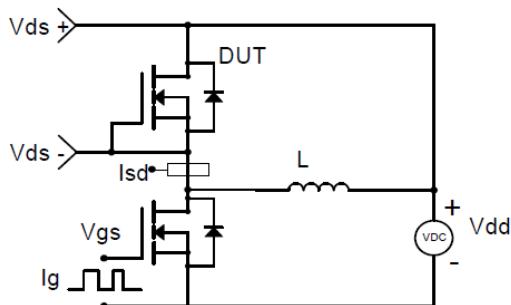
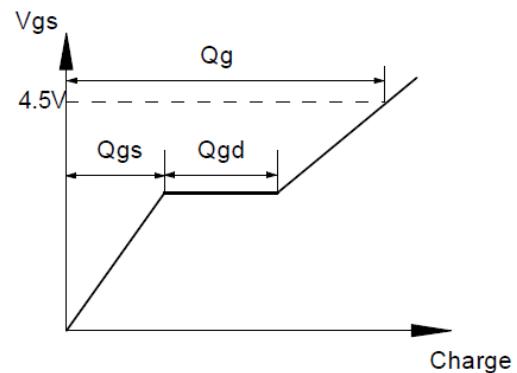
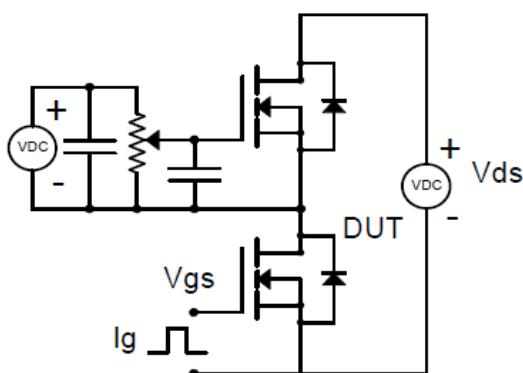
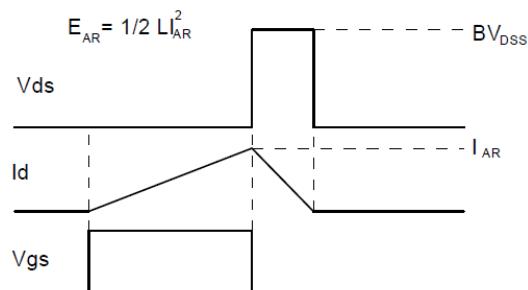
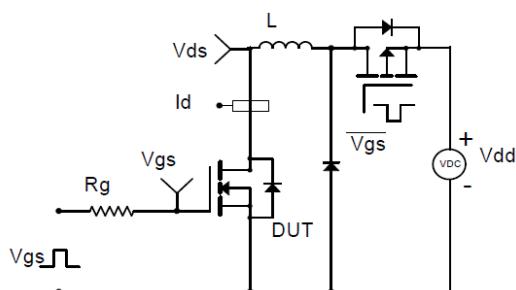
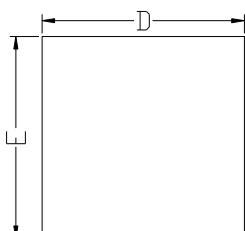


Figure 6. Gate Charge

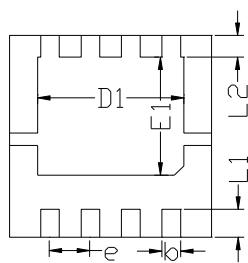

Figure 7. Safe Operation Area

Figure 8. Current dissipation

Figure 9. Normalized Threshold voltage

Figure 10. Normalized breakdown voltage

Figure 11. Normalized Maximum Transient Thermal Impedance


Resistive Switching Test Circuit & Waveforms

Diode Recovery Test Circuit & Waveforms

Gate Charge Test Circuit & Waveform

Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

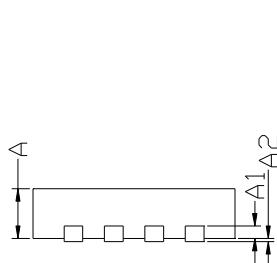
■DFN3333-8L Package information



Top View
正面视图



Bottom View
背面视图



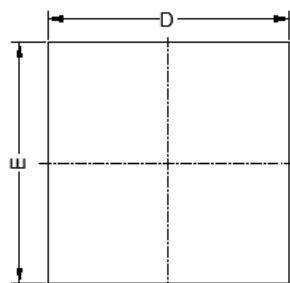
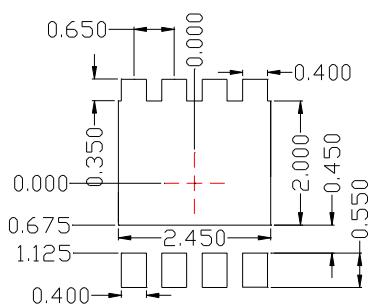
Side View
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20	BSC	
A2			0.10
D1	2.20	2.35	2.50
E1	1.80	1.90	2.00
L1	0.35	0.45	0.55
L2	0.35	BSC	
b	0.20	0.30	0.40
e	0.65	BSC	

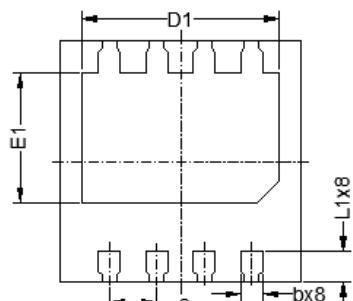
Note:

1. Controlling dimension:in millimeters.
2. General tolerance: $\pm 0.10\text{mm}$.
3. The pad layout is for reference purposes only.

Suggested Solder Pad Layout
Top View

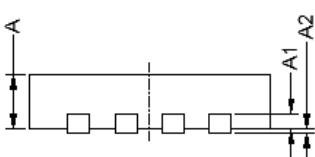


Top View
正面视图

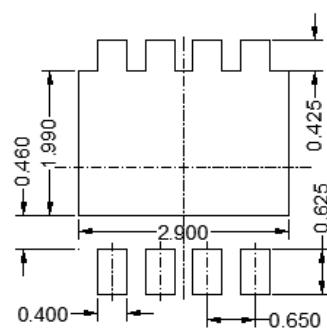


Bottom View
背面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D		3.30 BSC	
E		3.30 BSC	
A	0.70	0.75	0.80
A1	0.203	BSC	
A2			0.10
D1	2.55	2.70	2.80
E1	1.64	1.79	1.89
L1	0.325	0.425	0.525
b	0.20	0.30	0.40
e	0.65	BSC	



Side View
侧面视图



Note:

1. Controlling dimension:in millimeters.
2. General tolerance: $\pm 0.10\text{mm}$.
3. The pad layout is for reference purposes only.

Suggested Solder Pad Layout
Top View

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