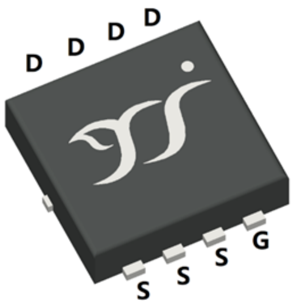
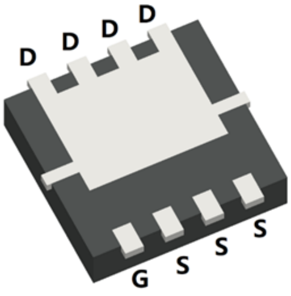
RoHS
COMPLIANT

N-Channel Enhancement Mode Field Effect Transistor

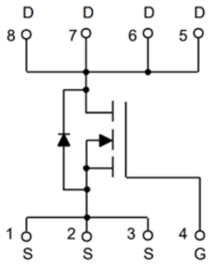


Top View



Bottom View

PDFN3333-8L



Product Summary

● V_{DS}	100V
● I_D	10A
● $R_{DS(ON)}$(at V_{GS}=10V)	＜120mΩ
● $R_{DS(ON)}$(at V_{GS}=4.5V)	＜130mΩ
● 100% EAS Tested	
● 100% ▽V_{DS} Tested	

General Description

- Trench Power MV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power management functions
- DC-DC convertor

■ Absolute Maximum Ratings (T_J=25℃ unless otherwise noted)

Parameter			Symbol	Limit	Unit
Drain-source Voltage			V_{DS}	100	V
Gate-source Voltage			V_{GS}	±20	V
Continuous Drain Current (Note 1,2)	Steady-State	T_A=25℃	I_D	2.6	A
		T_A=100℃		1.8	
Continuous Drain Current (Note 1,3)	Steady-State	T_C=25℃		10	
		T_C =100℃		7	
Pulsed Drain Current	T_C=25℃, t_p=100µs		I_{DM}	25	A
Avalanche energy	V_G=10V, R_G=25Ω, L=0.5mH, IAS=8.5A		EAS	18	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T_A=25℃	P_D	2.5	W
		T_A=100℃		1.25	
Total Power Dissipation (Note 1,3)	Steady-State	T_C=25℃		35	
		T_C =100℃		17	
Junction and Storage Temperature Range			T_J ,T_{STG}	-55～+175	℃

■Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	50	60	℃/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	3.5	4.2	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ120N10B	F1	Q120N10	5000	10000	100000	13“ reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V	-	-	1	μA
		V_{DS}=100V, V_{GS}=0V, Tj=125℃	-	-	100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.3	1.8	2.3	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=8A	-	90	120	mΩ
		V_{GS}=4.5V, I_D=6A	-	92	130	
Diode Forward Voltage	V_{SD}	I_S=10A, V_{GS}=0V	-	-	1.2	V
Gate resistance	R_G	f=1MHz	-	3.5	-	Ω
Maximum Body-Diode Continuous Current	I_S		-	-	10	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=50V, V_{GS}=0V, f=1MHz	-	998	-	pF
Output Capacitance	C_{oss}		-	28	-	
Reverse Transfer Capacitance	C_{rss}		-	22	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V, V_{DS}=50V, I_D=10A	-	19	-	nC
Gate-Source Charge	Q_{gs}		-	3	-	
Gate-Drain Charge	Q_{gd}		-	3.6	-	
Reverse Recovery Charge	Q_{rr}	I_F=10A, di/dt=100A/us	-	25	-	nC
Reverse Recovery Time	t_{rr}		-	27	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DD}=50V, I_D=10A R_{GEN}=2.2Ω	-	6.5	-	ns
Turn-on Rise Time	t_r		-	21	-	
Turn-off Delay Time	$t_{D(off)}$		-	21	-	
Turn-off fall Time	t_f		-	2.2	-	

Note:

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in^2 pad of 2oz. Copper, in the still air environment with TA =25℃.The maximum allowed junction temperature of 175℃. The value in any given application depends on the user's specific board design.
3. Thermal resistance from junction to soldering point (on the exposed drain pad).

■Typical Electrical and Thermal Characteristics Diagrams

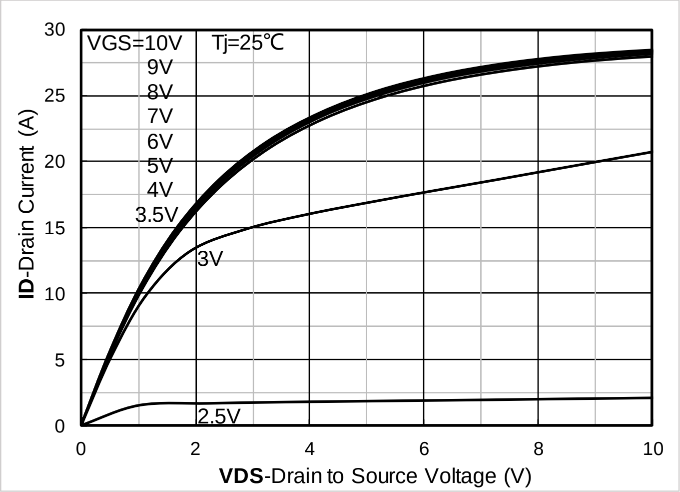


Figure 1. Output Characteristics

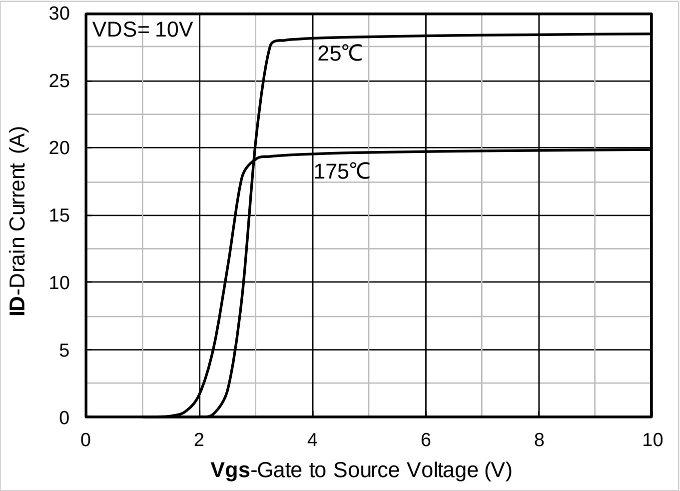


Figure 2. Transfer Characteristics

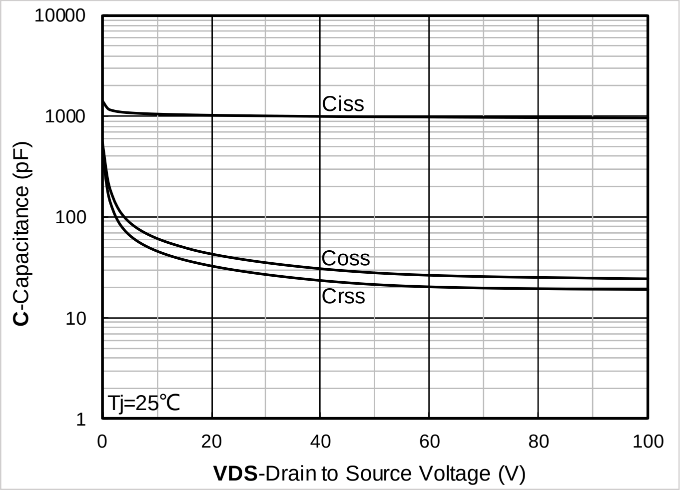


Figure 3. Capacitance Characteristics

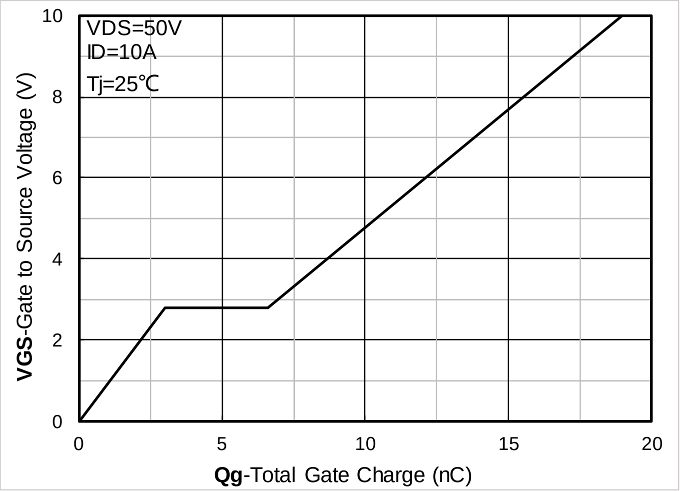


Figure 4. Gate Charge

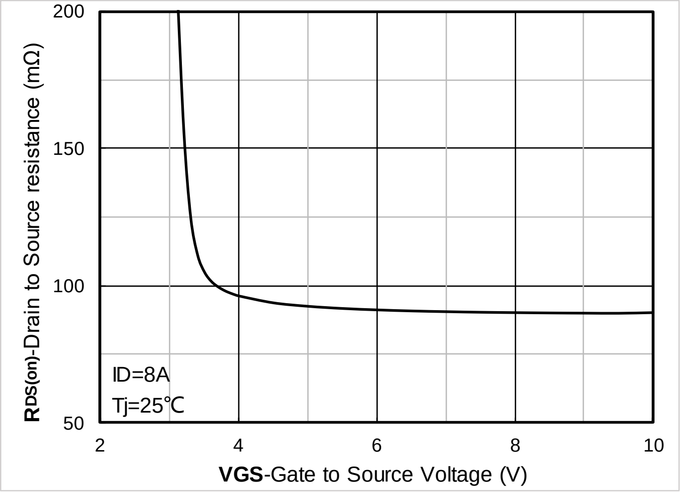


Figure 5. On-Resistance vs Gate to Source Voltage

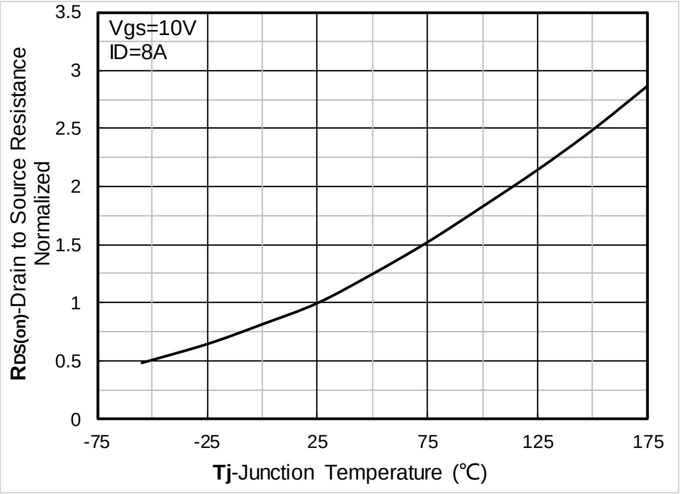


Figure 6. Normalized On-Resistance

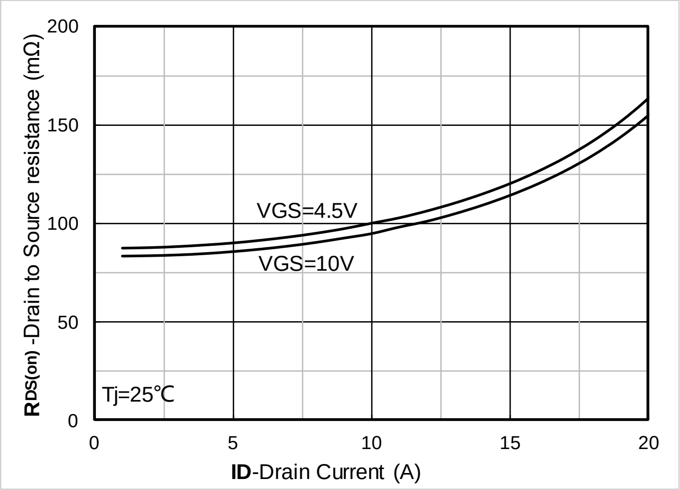


Figure 7. RDS(on) VS Drain Current

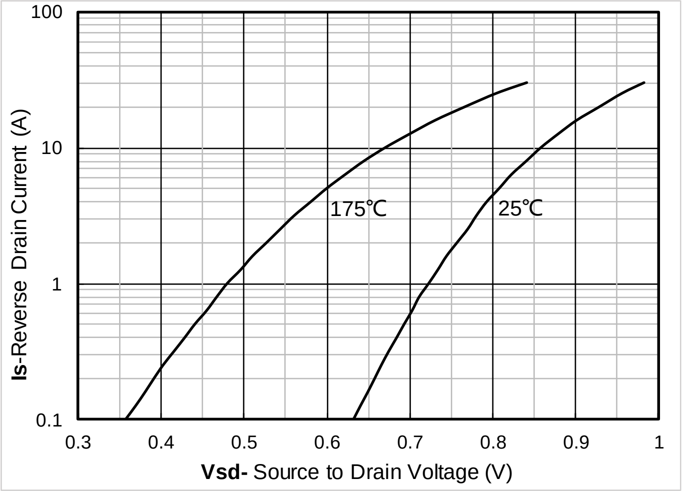


Figure 8. Forward characteristics of reverse diode

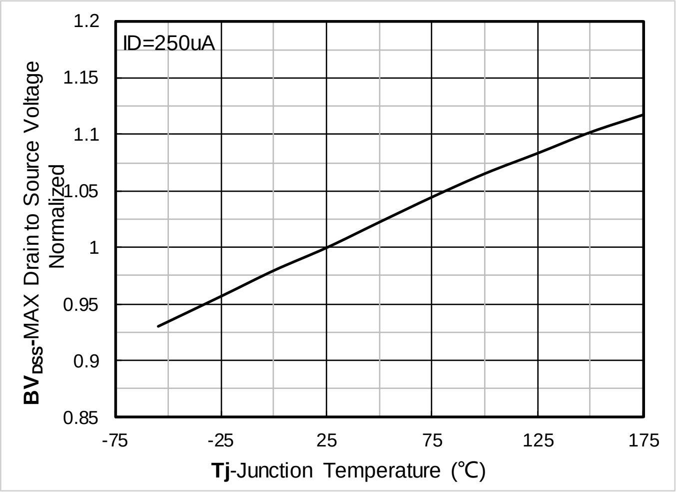


Figure 9. Normalized breakdown voltage

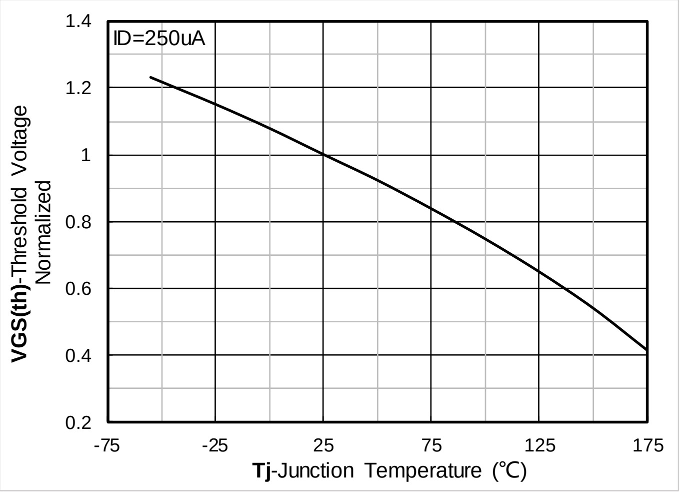


Figure 10. Normalized Threshold voltage

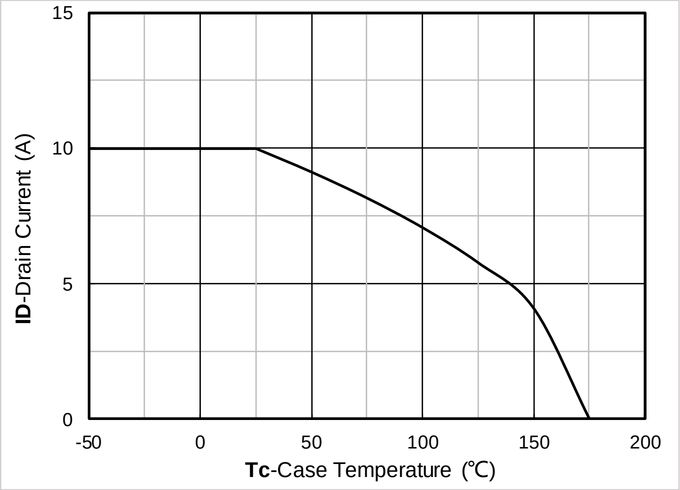


Figure 11. Current dissipation

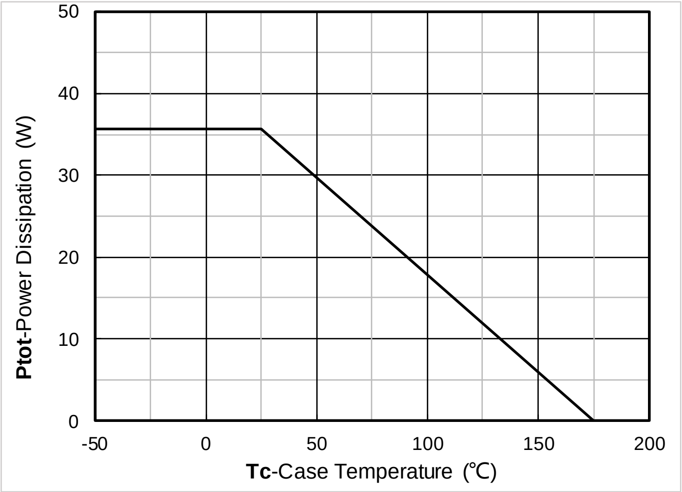


Figure 12. Power dissipation

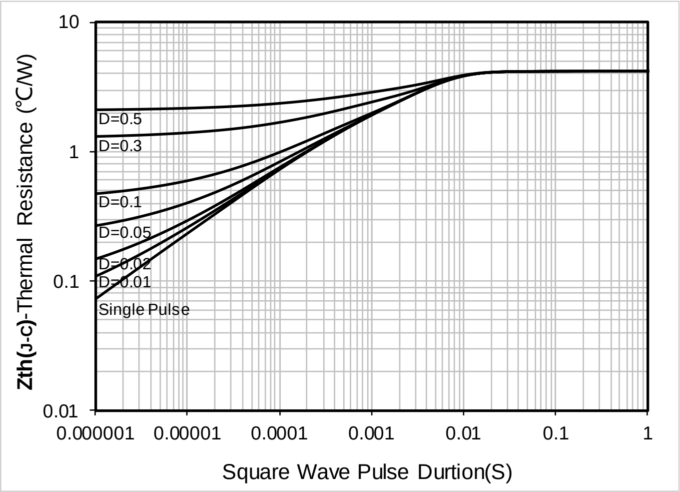


Figure 13. Maximum Transient Thermal Impedance

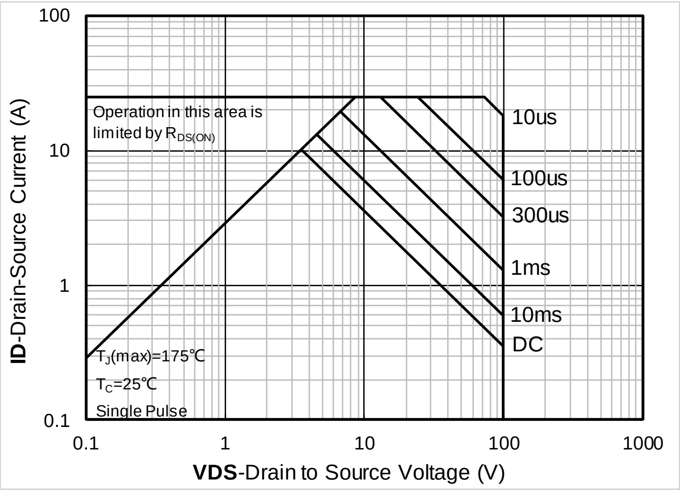


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

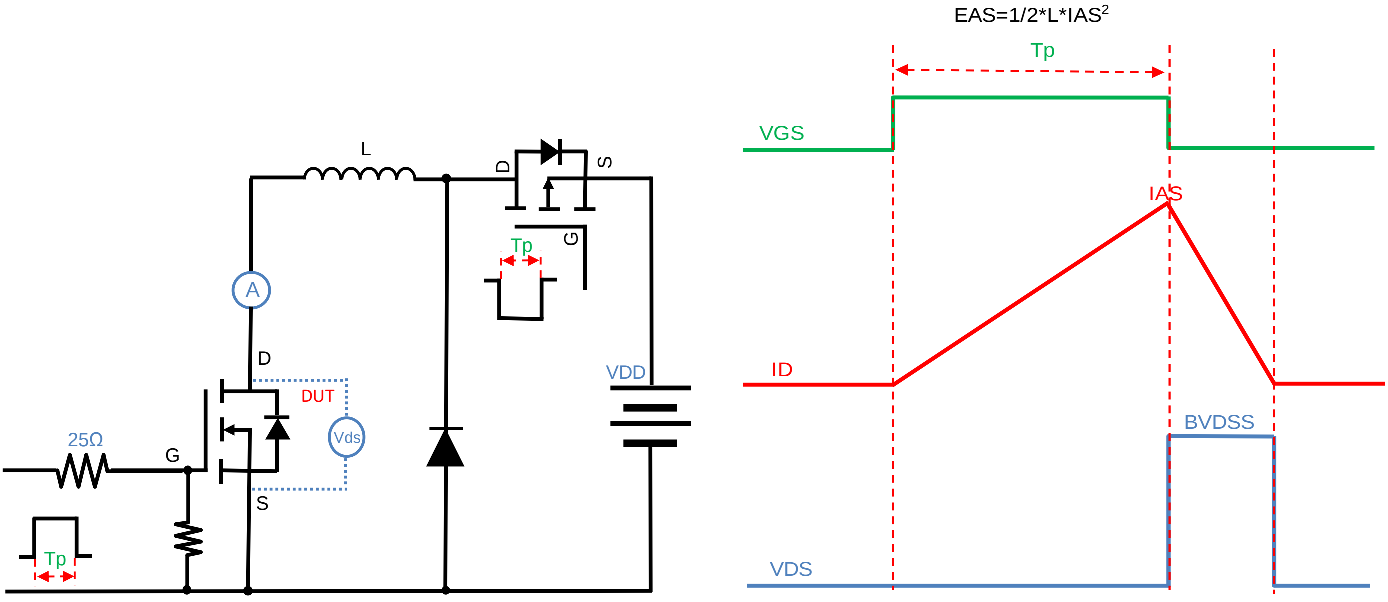


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

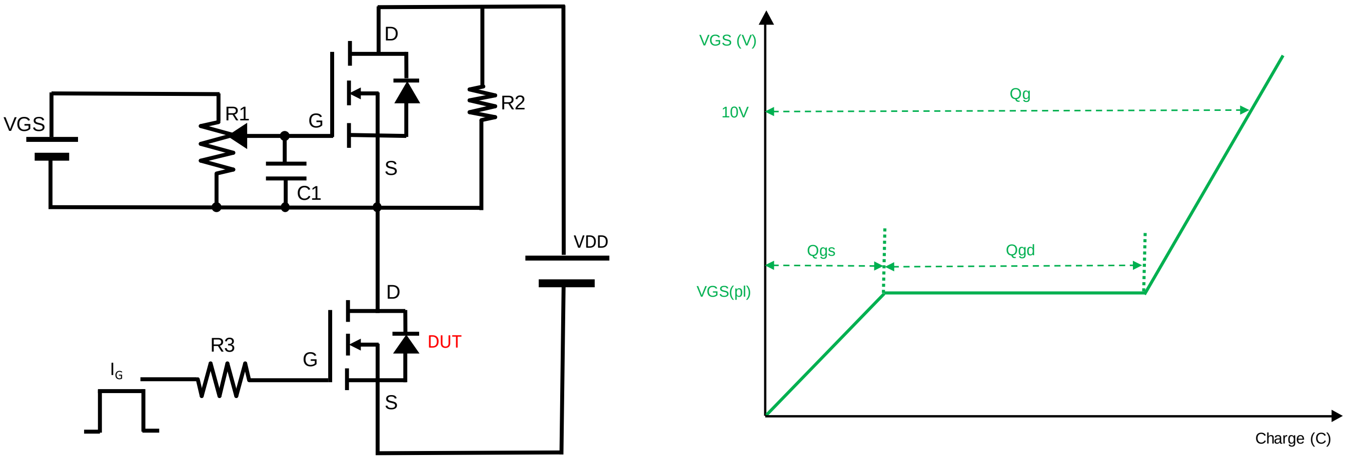


Figure B. Gate Charge Test Circuit & Waveform

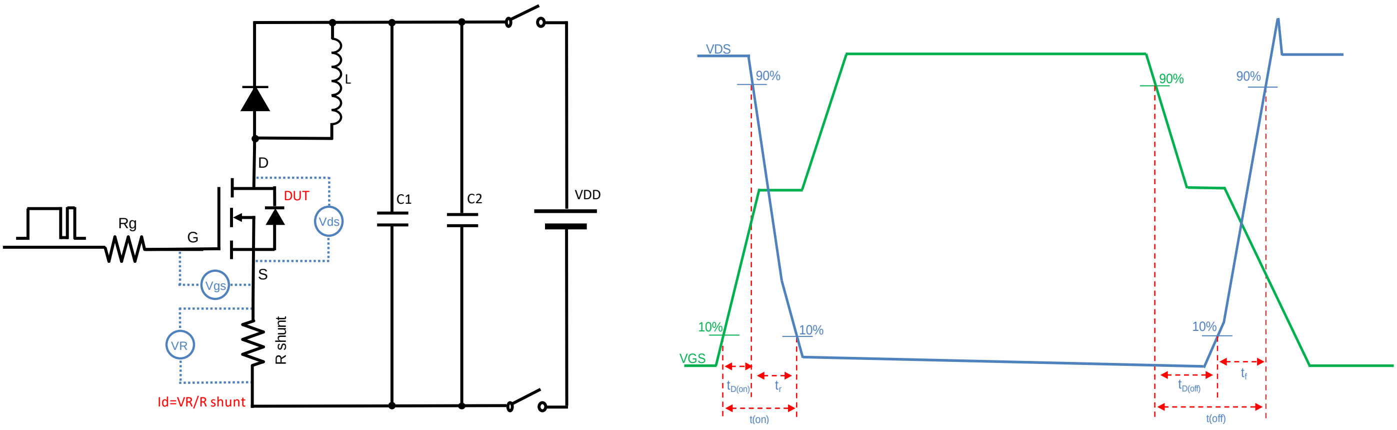


Figure C. Resistive Switching Test Circuit & Waveform

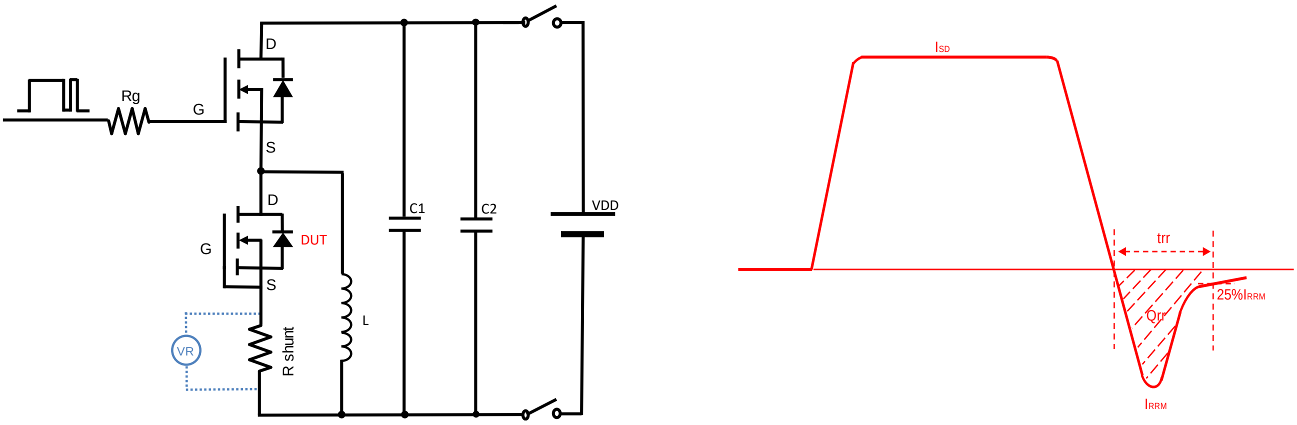
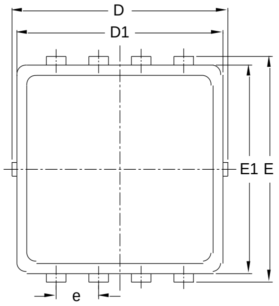
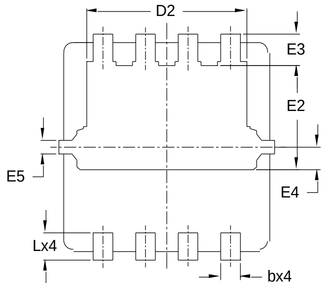


Figure D. Diode Recovery Test Circuit & Waveform

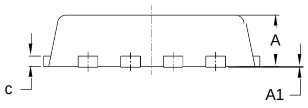
■ PDFN3333-8L-B-0.75mm Package information



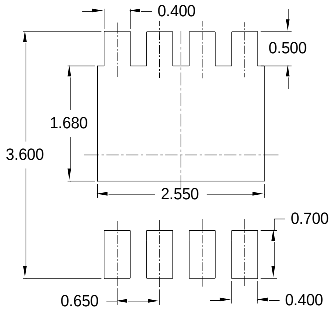
TOP VIEW



BOTTOM VIEW



SIDE VIEW



SUGGESTED SOLDER PAD LAYOUT

UNIT：mm

DIMENSIONS				
SYMBOL	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.028	0.033	0.700	0.850
A1	0.000	0.002	0.000	0.050
b	0.008	0.016	0.200	0.400
c	0.004	0.010	0.100	0.250
D	0.124	0.136	3.150	3.450
D1	0.118	0.130	3.000	3.300
D2	0.089	0.104	2.250	2.650
E	0.124	0.136	3.150	3.450
E1	0.114	0.126	2.900	3.200
E2	0.052	0.068	1.320	1.720
E3	0.011	0.026	0.280	0.650
E4	0.013 REF		0.330 REF	
E5	0.008 REF		0.200 REF	
e	0.026 BSC		0.650 BSC	
L	0.012	0.020	0.300	0.500

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

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