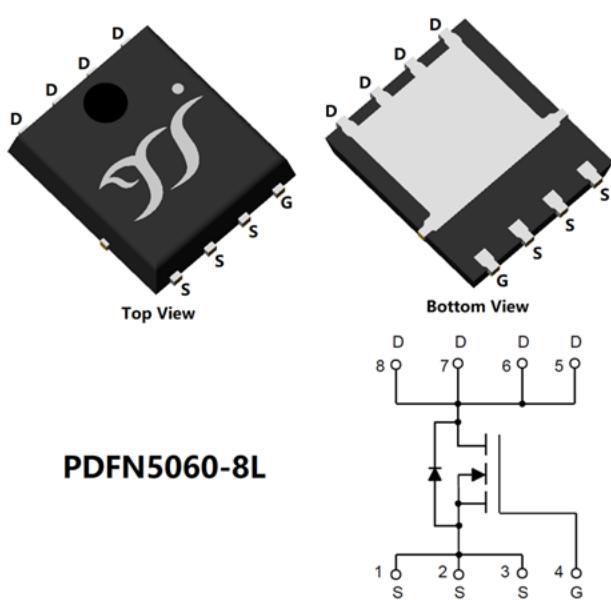




N-Channel Enhancement Mode Field Effect Transistor



Product Summary

- V_{DS} 60V
- I_D 50A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) $<9.5m\Omega$
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) $<14m\Omega$
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor

Absolute Maximum Ratings ($T_J=25^\circ C$ unless otherwise noted)

Parameter			Symbol	Limit	Unit
Drain-source Voltage			V_{DS}	60	V
Gate-source Voltage			V_{GS}	± 20	V
Continuous Drain Current (Note 1,2)	Steady-State	$T_A=25^\circ C$	I_D	11.6	A
		$T_A=100^\circ C$		7.3	
Continuous Drain Current (Note 1,3)	Steady-State	$T_C=25^\circ C$	I_D	50	A
		$T_C=100^\circ C$		31	
Pulsed Drain Current	$T_C=25^\circ C$, $t_p=100\mu s$		I_{DM}	180	A
Avalanche energy	$V_G=10V$, $R_G=25\Omega$, $L=0.5mH$, $I_{AS}=13A$		EAS	42.25	mJ
Total Power Dissipation (Note 1,2)	Steady-State	$T_A=25^\circ C$	P_D	2.2	W
		$T_A=100^\circ C$		0.9	
Total Power Dissipation (Note 1,3)	Steady-State	$T_C=25^\circ C$	P_D	50	W
		$T_C=100^\circ C$		20	
Junction and Storage Temperature Range	T_J, T_{STG}			-55~+150	°C

Thermal resistance

Parameter			Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State		$R_{\theta JA}$	45	55	°C/W
Thermal Resistance Junction-to-Case		Steady-State	$R_{\theta JC}$	2.1	2.5	

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG9D5G06A	F1	YJG9D5G06A	5000	10000	100000	13" reel



YJG9D5G06A

■ Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}}=60\text{V}, V_{\text{GS}}=0\text{V}$	-	-	1	μA
		$V_{\text{DS}}=60\text{V}, V_{\text{GS}}=0\text{V}, T_J=150^\circ\text{C}$	-	-	100	
Gate-Body Leakage Current	I_{GSS}	$V_{\text{GS}}= \pm 20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	± 100	nA
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	1.3	1.8	2.3	V
Static Drain-Source On-Resistance	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=25\text{A}$	-	7.4	9.5	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=13\text{A}$	-	10.7	14	
Diode Forward Voltage	V_{SD}	$I_{\text{S}}=25\text{A}, V_{\text{GS}}=0\text{V}$	-	-	1.2	V
Gate resistance	R_{G}	$f=1\text{MHz}$	-	2	-	Ω
Maximum Body-Diode Continuous Current	I_{S}		-	-	50	A
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{\text{DS}}=30\text{V}, V_{\text{GS}}=0\text{V}, f=1\text{MHz}$	-	875	-	pF
Output Capacitance	C_{oss}		-	300	-	
Reverse Transfer Capacitance	C_{rss}		-	15.5	-	
Switching Parameters						
Total Gate Charge	Q_{g}	$V_{\text{GS}}=10\text{V}, V_{\text{DS}}=30\text{V}, I_{\text{D}}=23\text{A}$	-	15.2	-	nC
Gate-Source Charge	Q_{gs}		-	3.2	-	
Gate-Drain Charge	Q_{gd}		-	3.4	-	
Reverse Recovery Charge	Q_{rr}	$I_{\text{F}}=23\text{A}, di/dt=100\text{A/us}$	-	9	-	nC
Reverse Recovery Time	t_{rr}		-	17.3	-	ns
Turn-on Delay Time	$t_{\text{D}(\text{on})}$	$V_{\text{GS}}=10\text{V}, V_{\text{DD}}=30\text{V}, I_{\text{D}}=23\text{A}$ $R_{\text{GEN}}=2.7\Omega$	-	9	-	ns
Turn-on Rise Time	t_{r}		-	51	-	
Turn-off Delay Time	$t_{\text{D}(\text{off})}$		-	20	-	
Turn-off fall Time	t_{f}		-	6	-	

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- The value of R_{GJA} is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with $TA = 25^\circ\text{C}$. The maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design.
- Thermal resistance from junction to soldering point (on the exposed drain pad).



■ Typical Electrical and Thermal Characteristics Diagrams

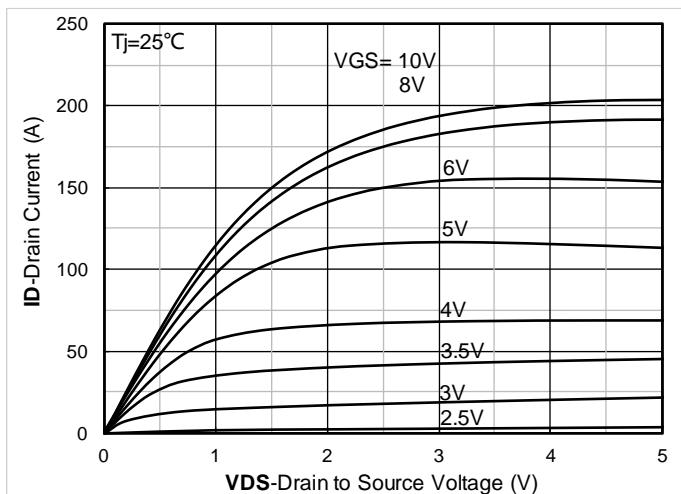


Figure 1. Output Characteristics

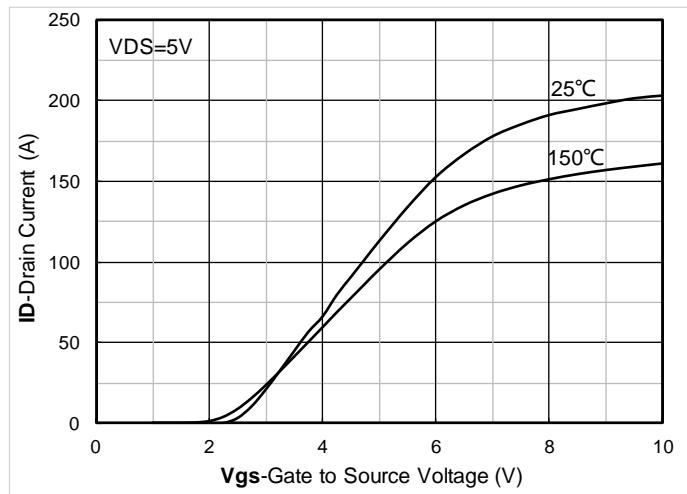


Figure 2. Transfer Characteristics

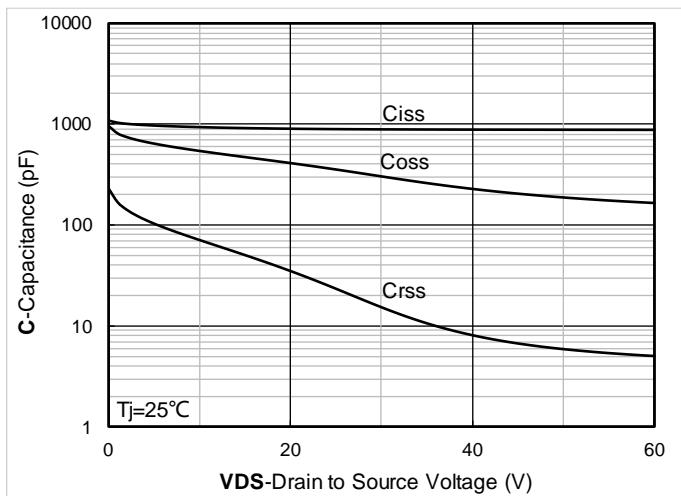


Figure 3. Capacitance Characteristics

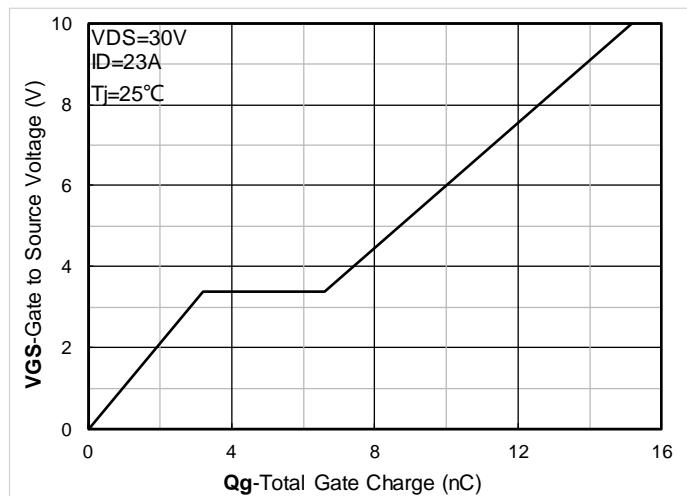


Figure 4. Gate Charge

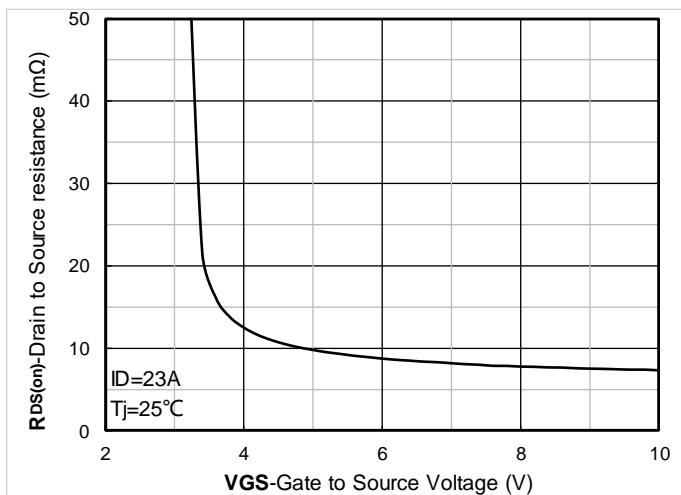


Figure 5. On-Resistance vs Gate to Source Voltage

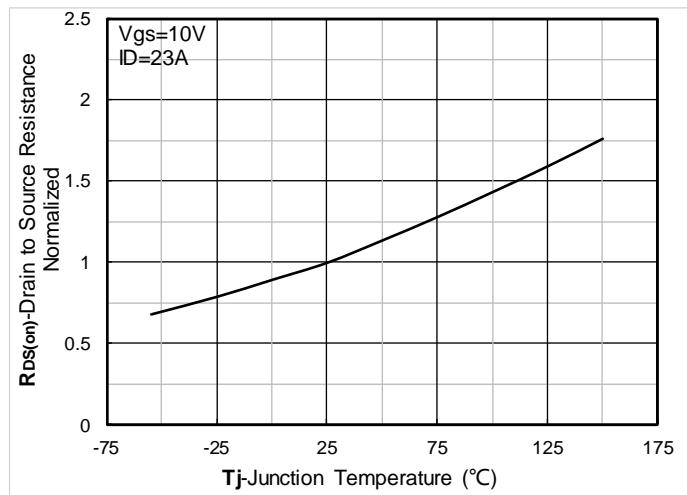


Figure 6. Normalized On-Resistance

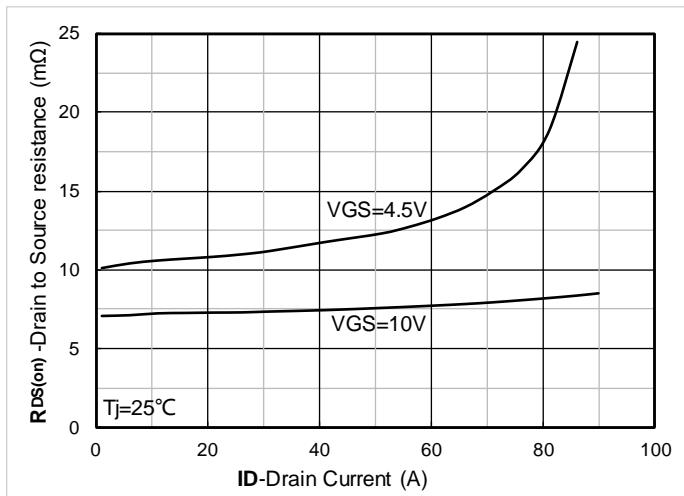
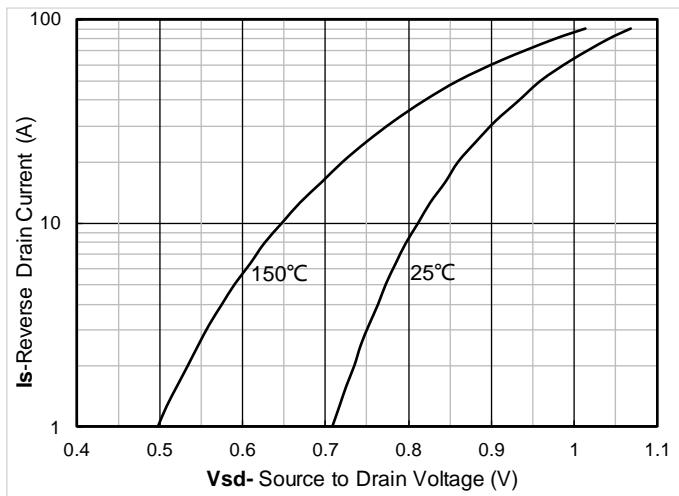
Figure 7. $R_{DS(on)}$ VS Drain Current

Figure 8. Forward characteristics of reverse diode

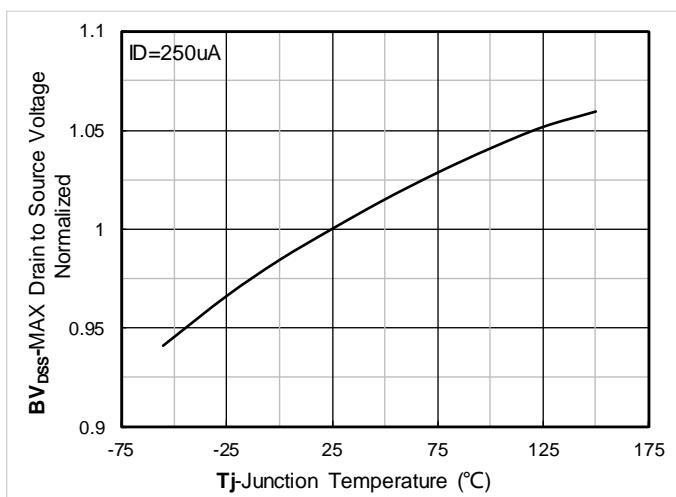


Figure 9. Normalized breakdown voltage

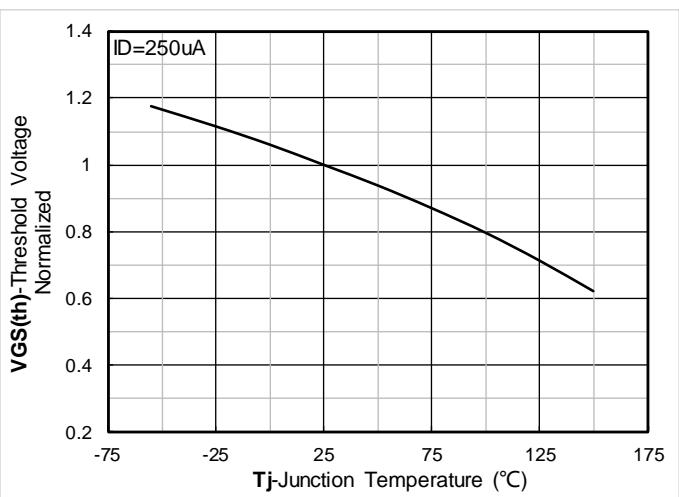


Figure 10. Normalized Threshold voltage

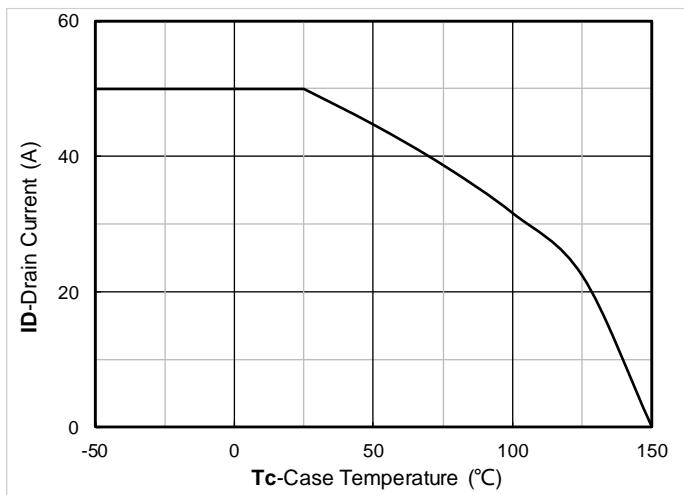


Figure 11. Current dissipation

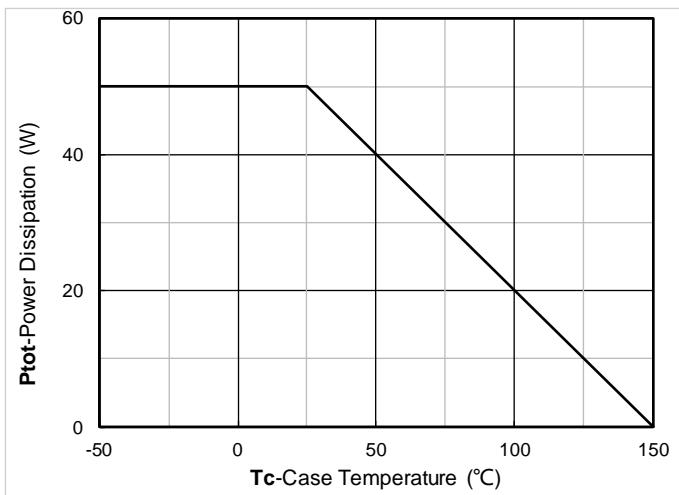


Figure 12. Power dissipation

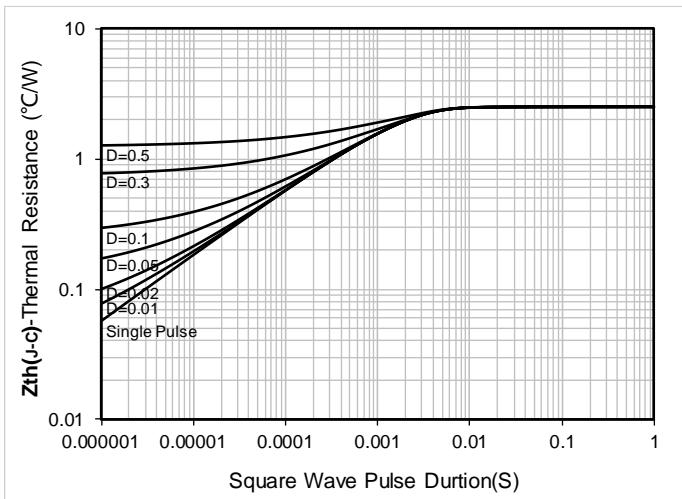


Figure 13. Maximum Transient Thermal Impedance

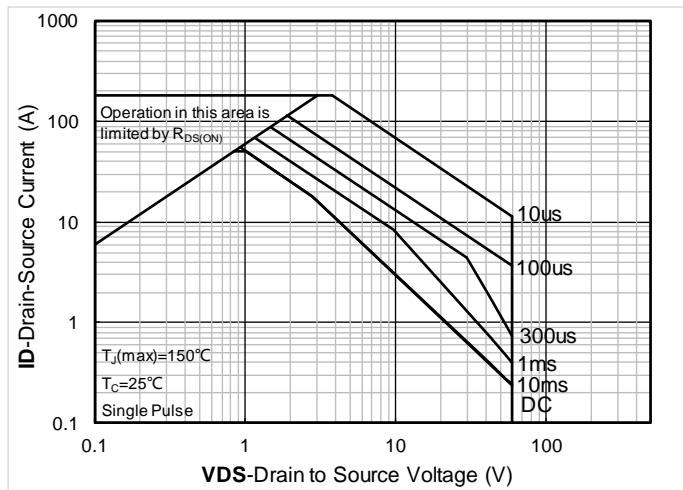


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

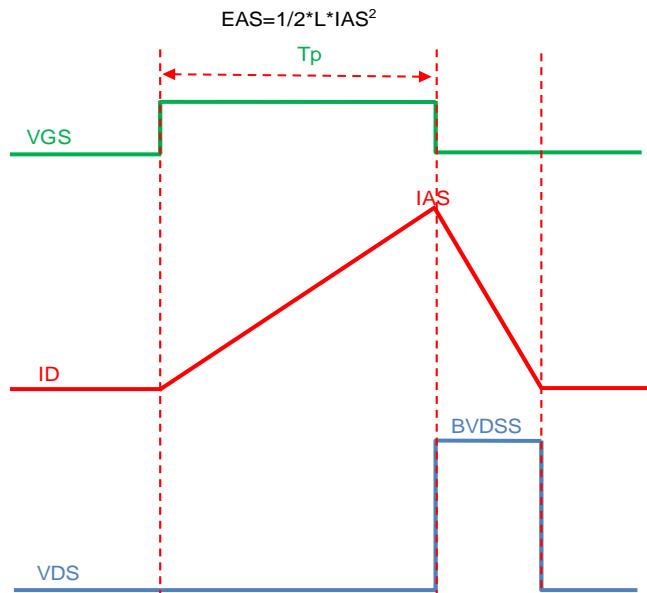
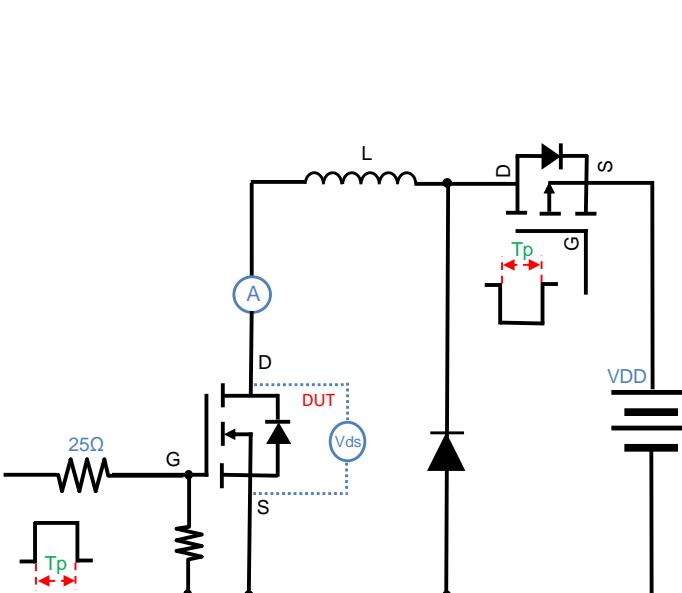


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

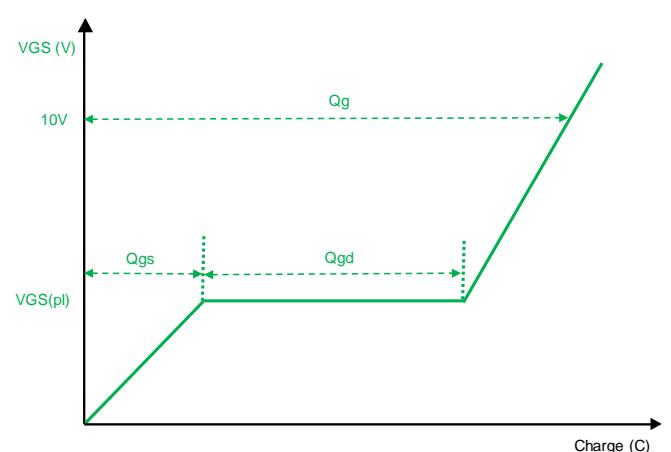
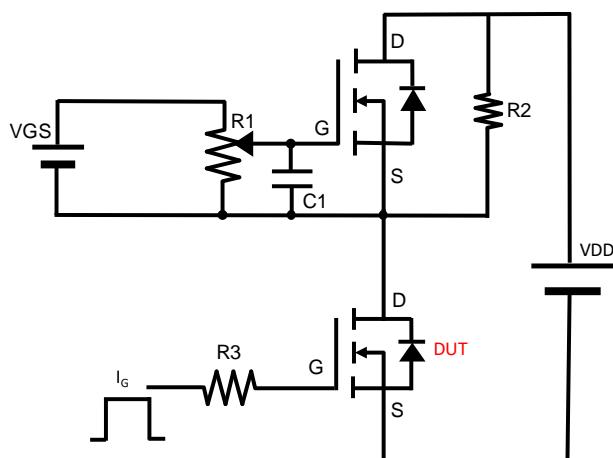


Figure B. Gate Charge Test Circuit & Waveform

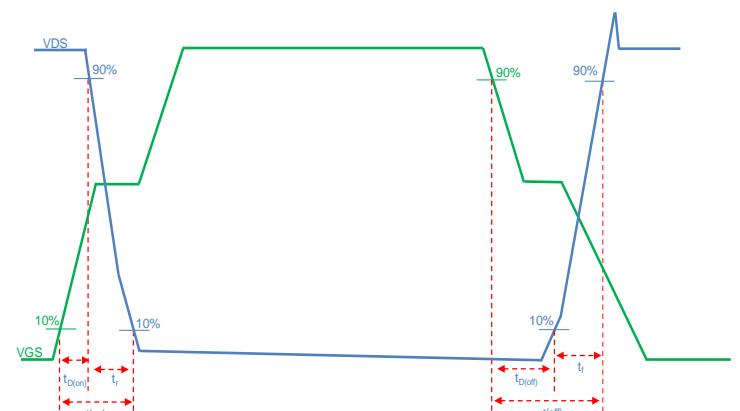
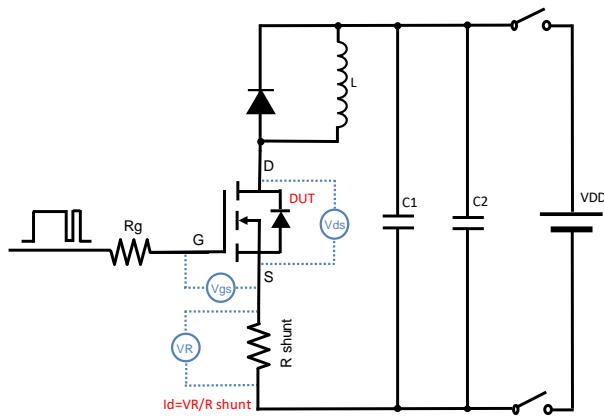


Figure C. Resistive Switching Test Circuit & Waveform

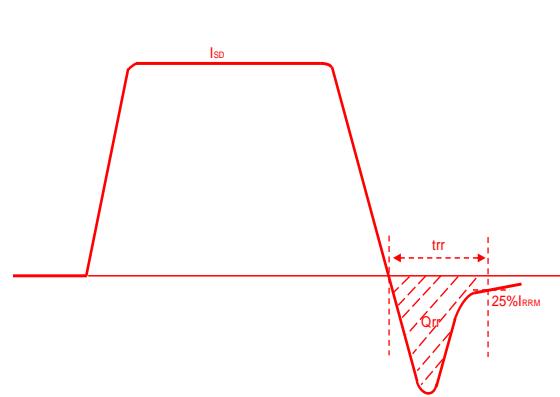
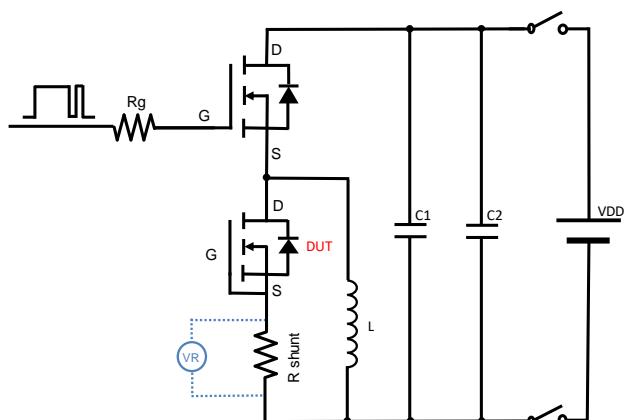
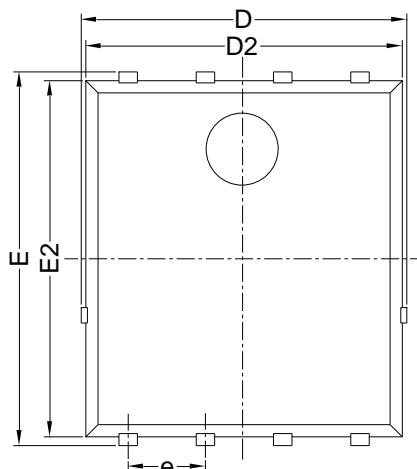
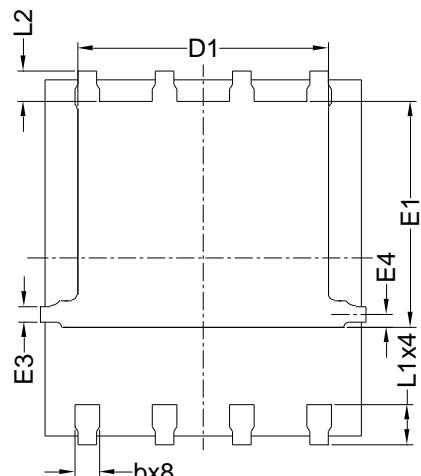
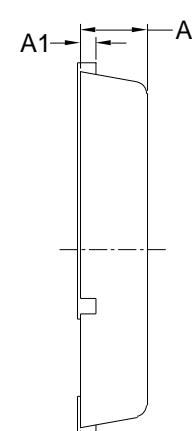
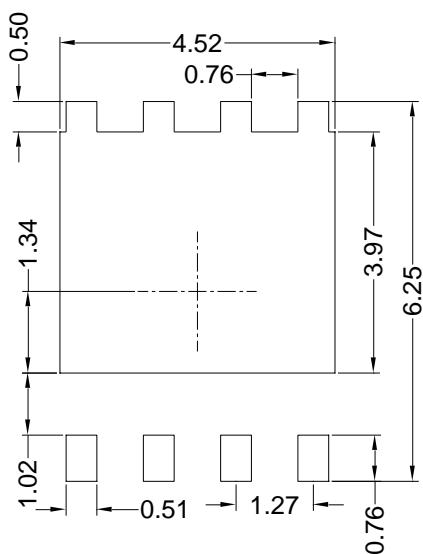


Figure D. Diode Recovery Test Circuit & Waveform



■ PDFN5060-8L-B-1.1MM Package information

Top View
正面视图Bottom View
背面视图Side View
侧面视图Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3	0.254 REF		
E4	0.21 REF		
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		

Note:

1. Controlling dimension:in millimeters.
2. General tolerance: $\pm 0.10\text{mm}$.
3. The pad layout is for reference purposes only.



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