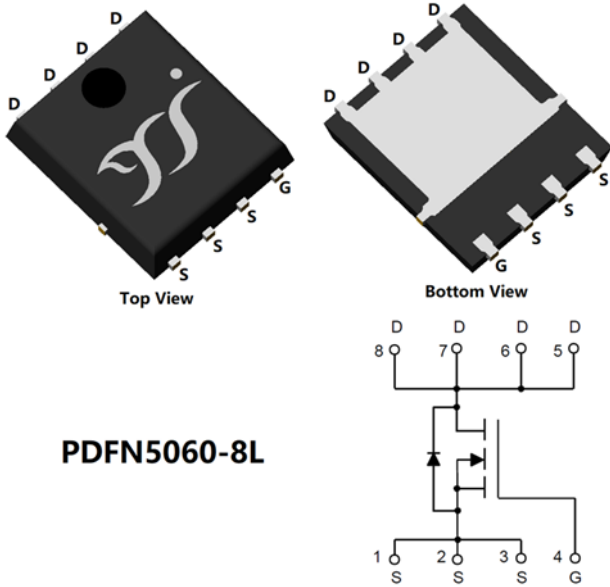


N-Channel Enhancement Mode Field Effect Transistor



PDFN5060-8L

Product Summary

- V_{DS} 60V
- I_D 20A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) <43mohm
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) <47mohm
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Trench Power MV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for Low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- DC-DC Converters
- Power management functions
- Backlighting

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_C=25^\circ\text{C}$	I_D	20	A
	$T_C=100^\circ\text{C}$		12.5	
Pulsed Drain Current ^A		I_{DM}	60	A
Total Power Dissipation @ $T_C=25^\circ\text{C}$		P_D	21	W
Single Pulse Avalanche Energy ^B		E_{AS}	20	mJ
Thermal Resistance Junction-to-Case		$R_{\theta JC}$	5.9	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction-to-Ambient ^C		$R_{\theta JA}$	57	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ\text{C}$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG20N06A	F1	YJG20N06A	5000	10000	100000	13" reel



YJG20N06A

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	60			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V,V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D =20A		34	43	mΩ
		V _{GS} = 4.5V, I _D =10A		36	47	
Diode Forward Voltage	V _{SD}	I _S =10A,V _{GS} =0V		0.8	1.2	V
Maximum Body-Diode Continuous Current	I _S				20	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =30V,V _{GS} =0V,f=1MHZ		1018		pF
Output Capacitance	C _{oss}			70		
Reverse Transfer Capacitance	C _{rss}			62		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V,V _{DS} =30V,I _D =10A		26		nC
Gate-Source Charge	Q _{gs}			5.4		
Gate-Drain Charge	Q _{gd}			6.5		
Reverse Recovery Chrage	Q _{rr}	I _F =20A, di/dt=500A/us		11.7		ns
Reverse Recovery Time	t _{rr}			23		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V,V _{DD} =30V, I _D =2A,R _L =1Ω R _{GEN} =3Ω		10		
Turn-on Rise Time	t _r			20		
Turn-off Delay Time	t _{D(off)}			29		
Turn-off fall Time	t _f			22		

A. Pulse Test: Pulse Width≤300us, Duty cycle ≤2%.

B. T_J=25℃, V_G=10V, R_G=25Ω, L=1mH, I_{AS}=8A.

C. The value of R_{θJA} is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with T_A=25℃. The maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design.



■ Typical Performance Characteristics

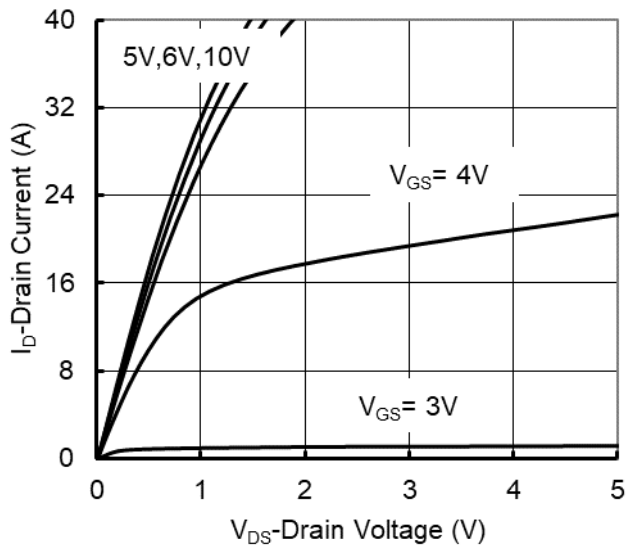


Figure 1. Output Characteristics

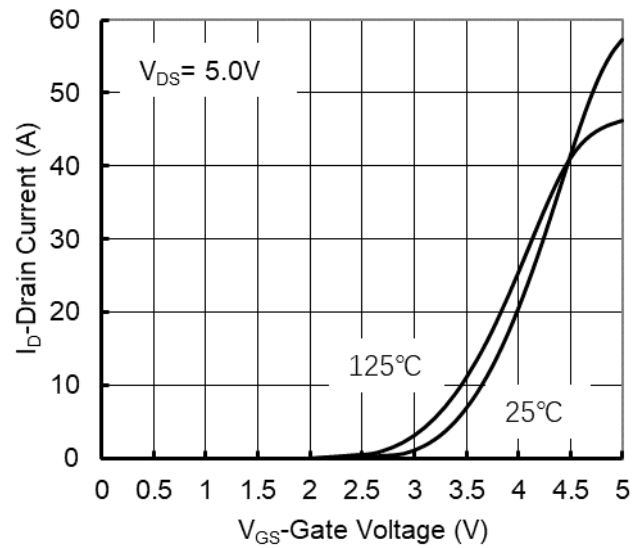


Figure 2. Transfer Characteristics

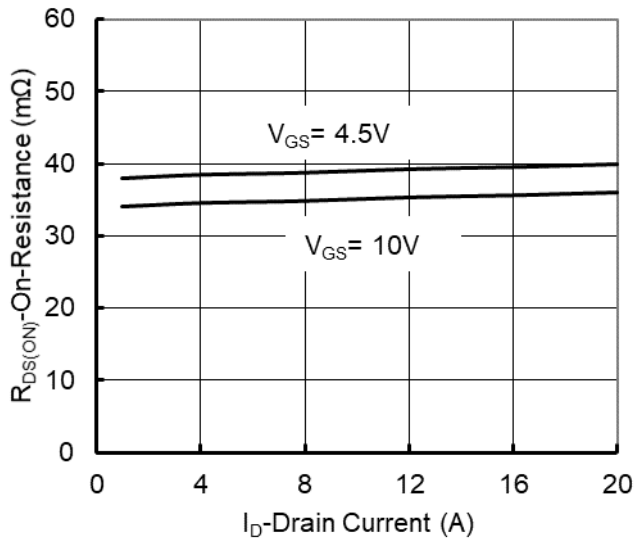


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

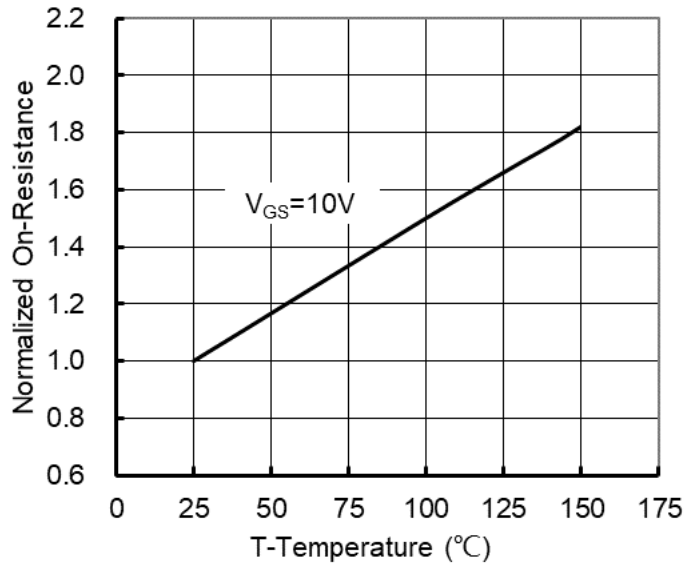


Figure 4. On-Resistance vs. Junction Temperature

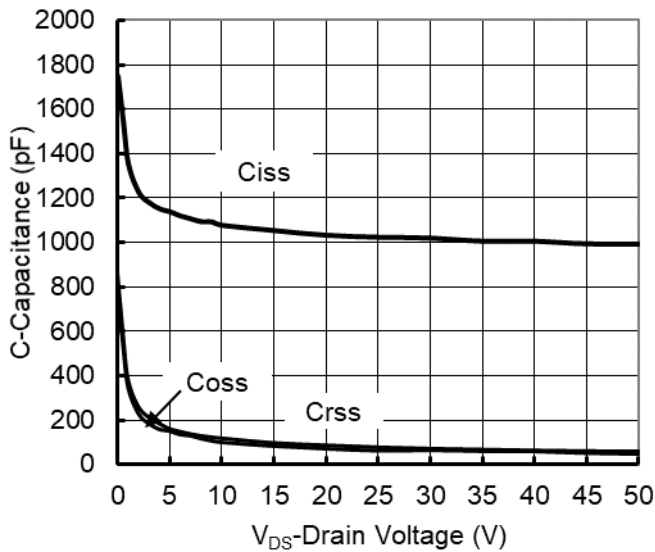


Figure 5. Capacitance Characteristics

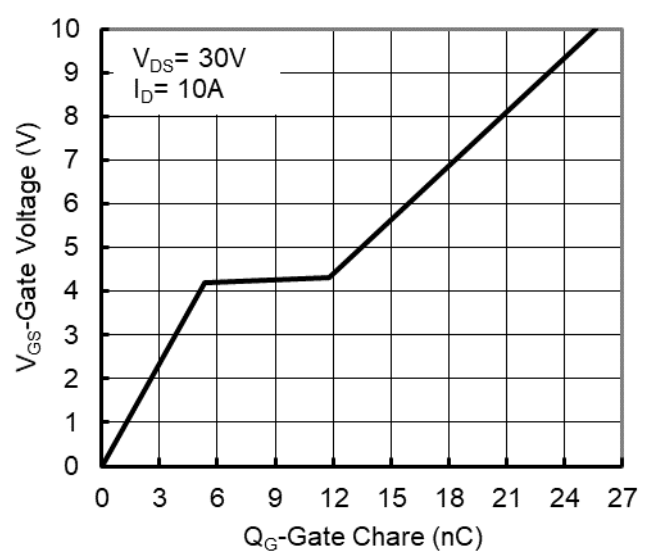


Figure 6. Gate Charge

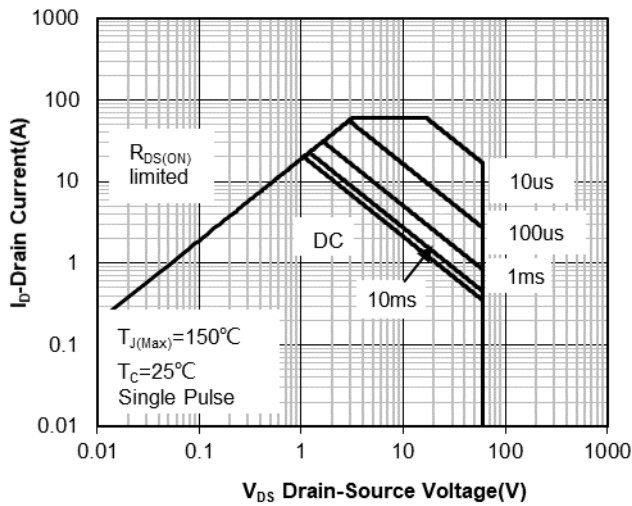


Figure 7. Safe Operation Area

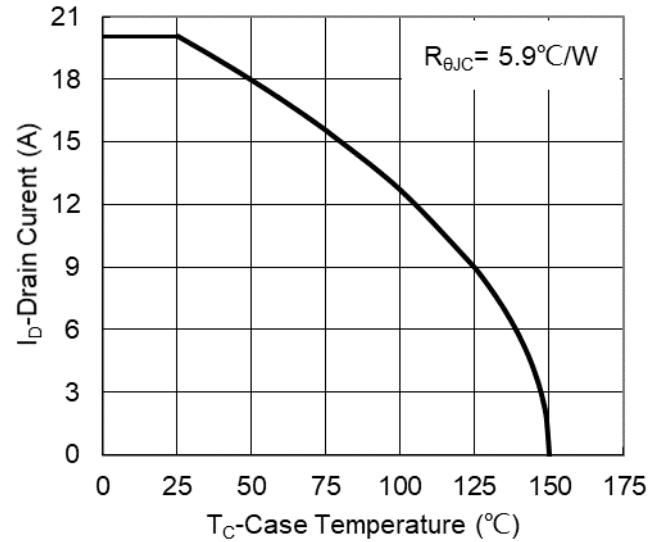


Figure 8. Maximum Continuous Drain Current vs Case Temperature

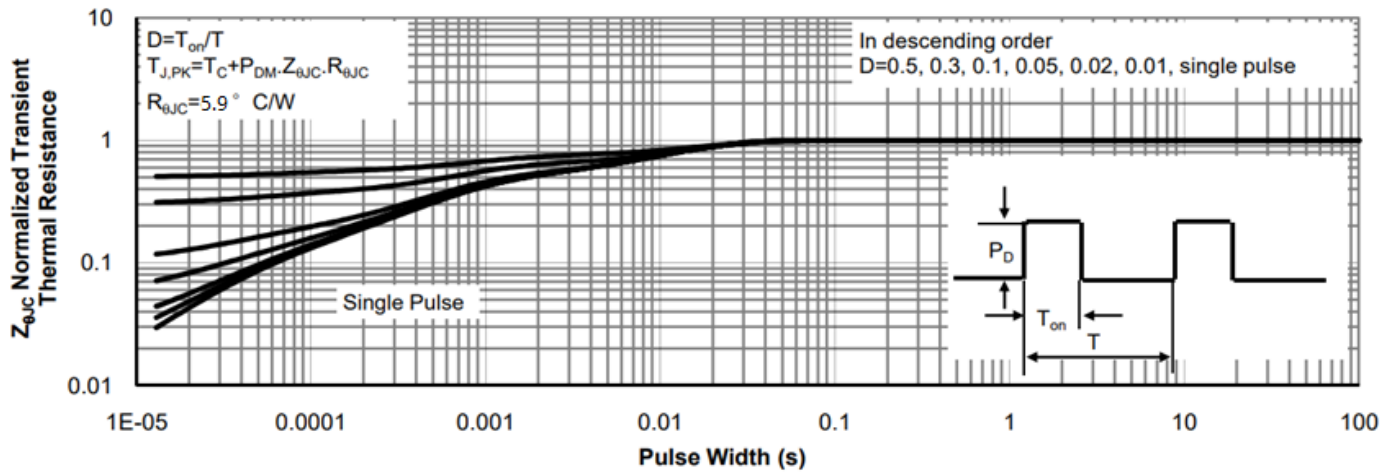
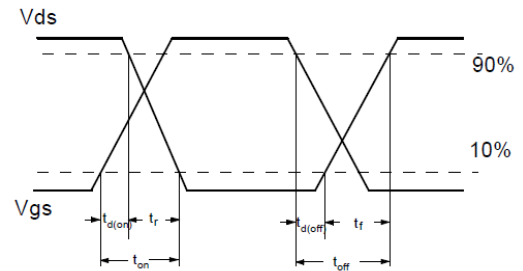
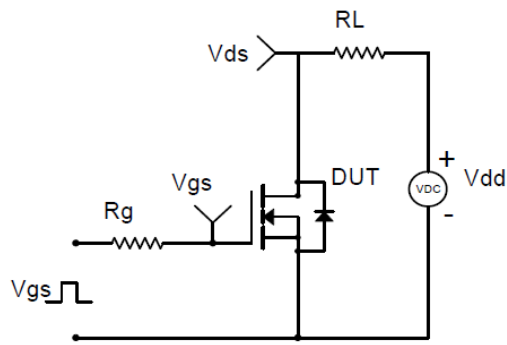
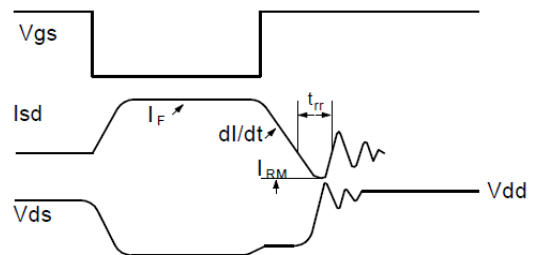
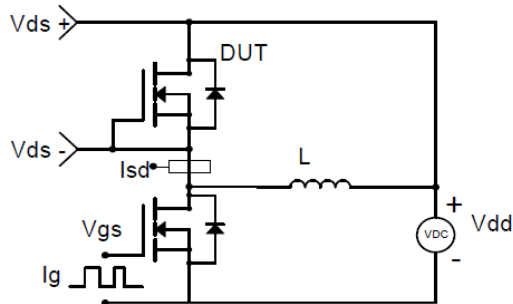


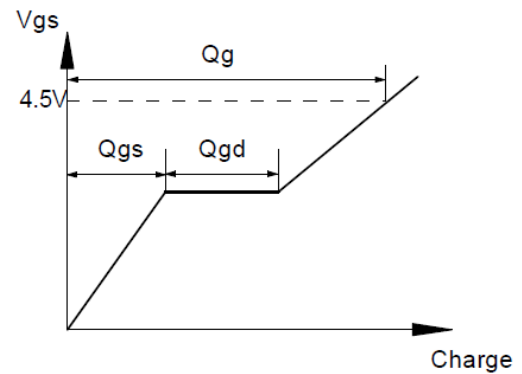
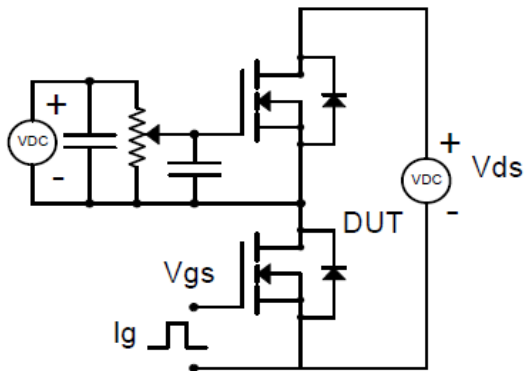
Figure 9. Normalized Maximum Transient Thermal Impedance



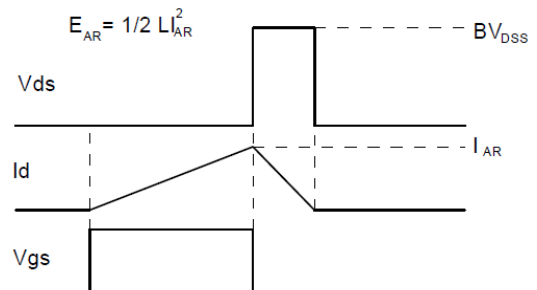
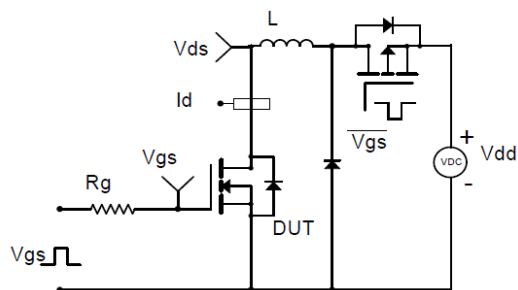
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform

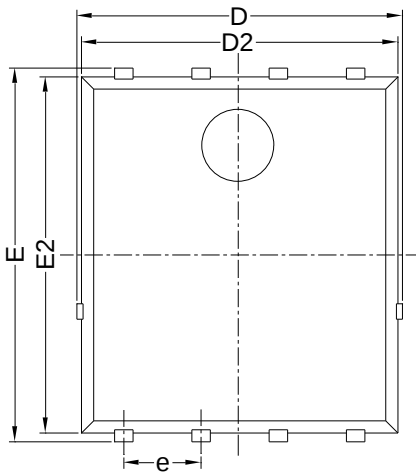


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

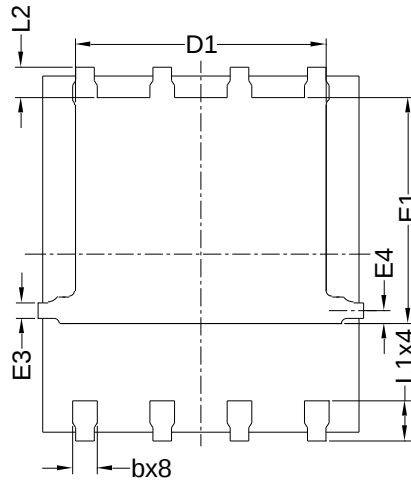


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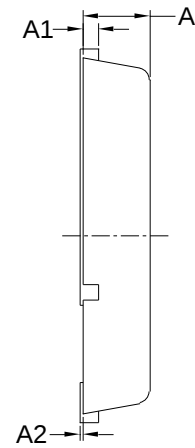
■ PDFN5060-8L-B-1.1MM Package Information



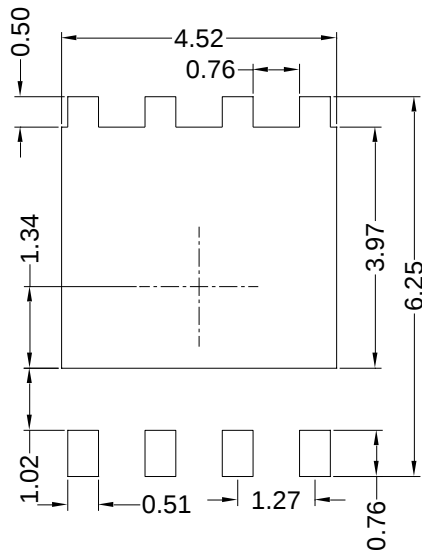
Top View
正面视图



Bottom View
背面视图



Side View
侧面视图



Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3	0.254 REF		
E4	0.21 REF		
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.10\text{mm}$.
3. The pad layout is for reference purposes only.



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