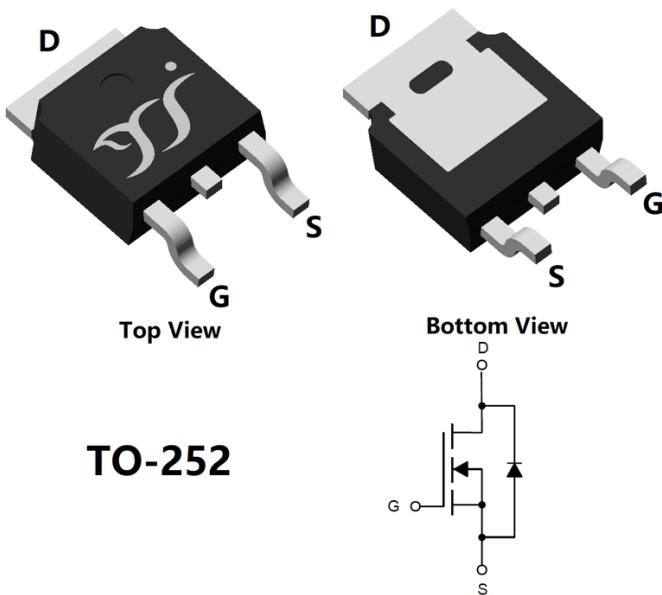




N-Channel Enhancement Mode Field Effect Transistor



Product Summary

- V_{DS} 60 V
- I_D 90 A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) <7.2 mohm
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) <8.5 mohm
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Trench Power MV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- DC-DC Converters
- Power management functions
- Motor Drive applications

■ Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_c=25^\circ C$	I_D	90	A
	$T_c=100^\circ C$		57	
Pulsed Drain Current ^A		I_{DM}	300	A
Total Power Dissipation @ $T_c=25^\circ C$ ^B		P_D	110	W
Total Power Dissipation @ $T_c=100^\circ C$ ^B		P_D	44	W
Total Power Dissipation @ $T_A=25^\circ C$ ^C		P_D	6.2	W
Single Pulse Avalanche Energy ^D		E_{AS}	196	mJ
Thermal Resistance Junction-to-Case		$R_{\theta JC}$	1.14	$^\circ C/W$
Thermal Resistance Junction-to-Ambient		$R_{\theta JA}$	20	$^\circ C/W$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ C$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJD90N06A	F1/F2	YJD90N06A	2500	/	25000	13" reel



YJD90N06A

■ Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	60			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}}=60\text{V}, V_{\text{GS}}=0\text{V}$			1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{\text{GS}}= \pm 20\text{V}, V_{\text{DS}}=0\text{V}$			± 100	nA
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}}= 10\text{V}, I_{\text{D}}=45\text{A}$		5.8	7.2	$\text{m}\Omega$
		$V_{\text{GS}}= 10\text{V}, I_{\text{D}}=15\text{A}$		5.6	7.2	
		$V_{\text{GS}}= 4.5\text{V}, I_{\text{D}}=10\text{A}$		6.8	8.5	
Diode Forward Voltage	V_{SD}	$I_{\text{S}}=45\text{A}, V_{\text{GS}}=0\text{V}$		0.90	1.2	V
Maximum Body-Diode Continuous Current	I_{S}				90	A
Gate resistance	R_g	$f=1\text{ MHz}, \text{Open drain}$		2.1		Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{\text{DS}}=30\text{V}, V_{\text{GS}}=0\text{V}, f=1\text{MHz}$		5170		pF
Output Capacitance	C_{oss}			300		
Reverse Transfer Capacitance	C_{rss}			155		
Switching Parameters						
Total Gate Charge	$Q_g(10\text{V})$	$V_{\text{GS}}=10\text{V}, V_{\text{DS}}=30\text{V}, I_{\text{D}}=20\text{A}$		102		nC
Total Gate Charge	$Q_g(4.5\text{V})$			48		
Gate-Source Charge	Q_{gs}			18.7		
Gate-Drain Charge	Q_{gd}			20		
Reverse Recovery Charge	Q_{rr}	$I_{\text{F}}=20\text{A}, \text{di/dt}=100\text{A/us}$		18		ns
Reverse Recovery Time	t_{rr}			27		
Turn-on Delay Time	$t_{\text{D(on)}}$			12		
Turn-on Rise Time	t_r	$V_{\text{GS}}=10\text{V}, V_{\text{DD}}=30\text{V}, I_{\text{D}}=20\text{A}$ $R_{\text{GEN}}=3\Omega$		46		ns
Turn-off Delay Time	$t_{\text{D(off)}}$			90		
Turn-off fall Time	t_f			80		

- A. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.
- B. The power dissipation P_D is based on $T_{J(\text{MAX})}=150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- C. The value of $R_{\theta JA}$ is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$.
- D. $T_J=25^\circ\text{C}$, $V_{\text{DD}}=55\text{V}$, $V_G=10\text{V}$, $L=0.5\text{mH}$.



■ Typical Performance Characteristics

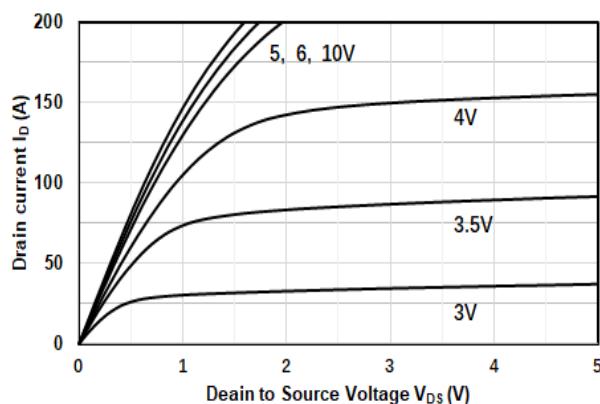


Figure1. Output Characteristics

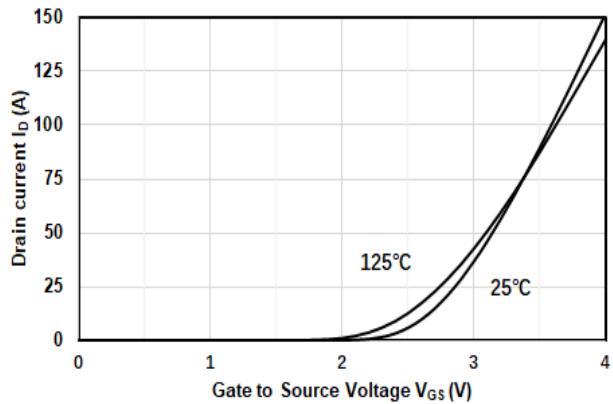


Figure2. Transfer Characteristics

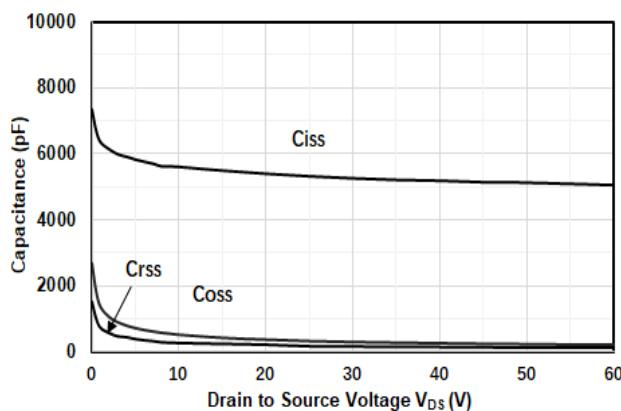


Figure3. Capacitance Characteristics

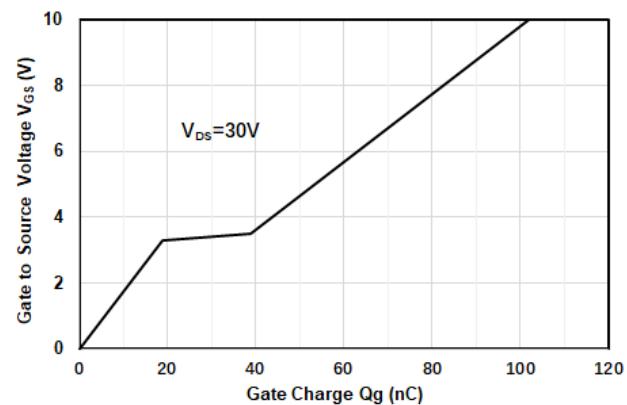


Figure4. Gate Charge

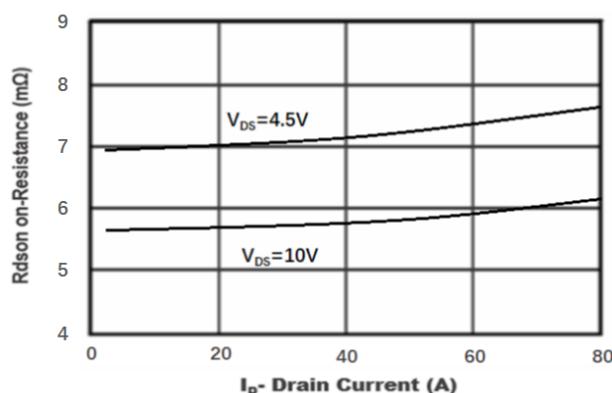


Figure5. Drain-Source on Resistance

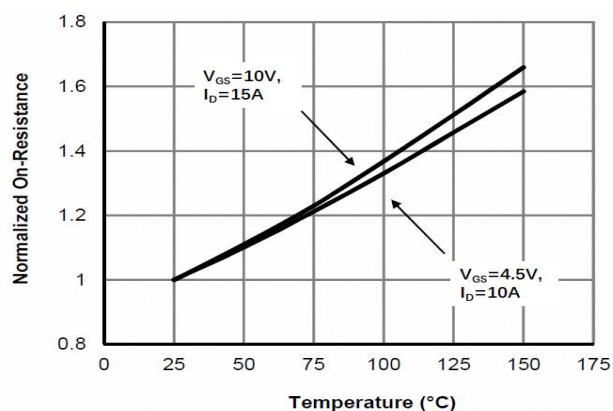


Figure6. Drain-Source on Resistance



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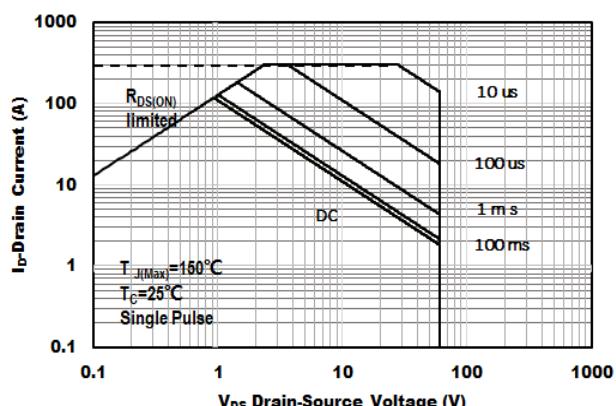


Figure 7. Safe Operation Area

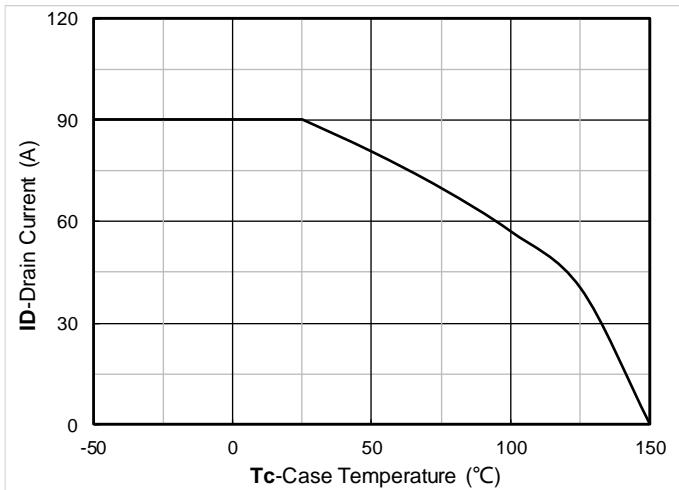


Figure 8. Current dissipation

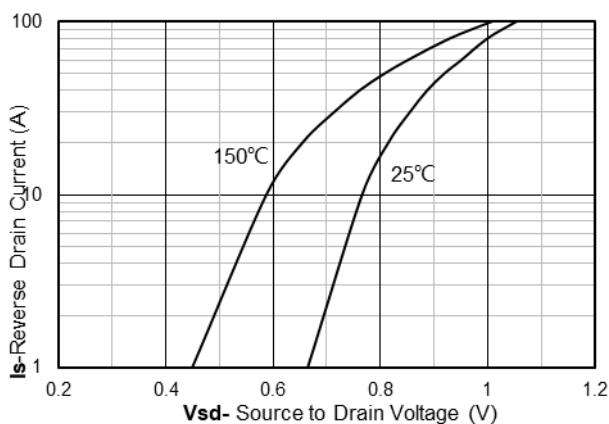


Figure 9. Forward characteristics of reverse diode

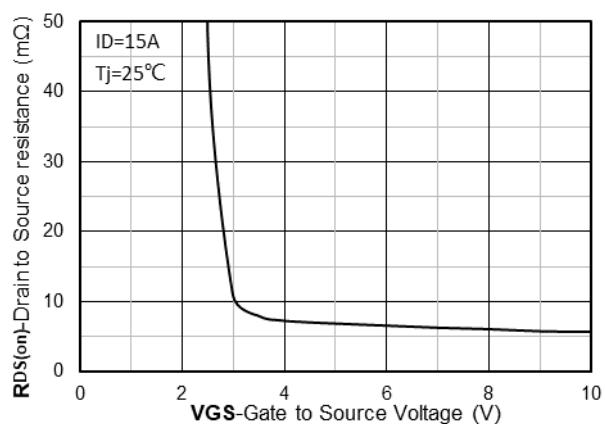


Figure 10. On-Resistance vs Gate to Source Voltage

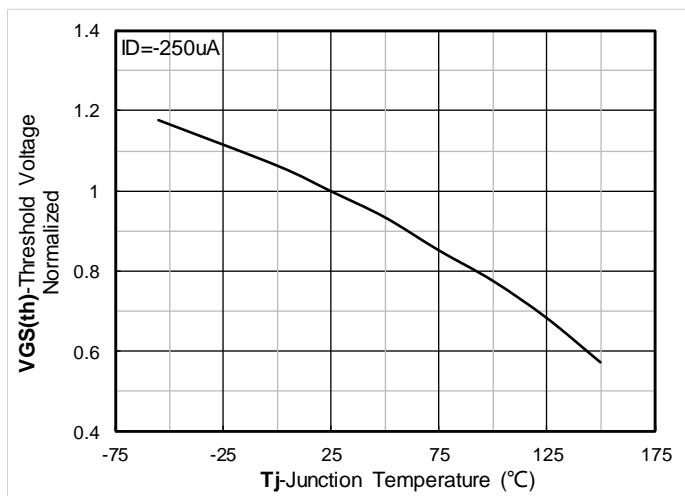


Figure 11. Normalized Threshold voltage

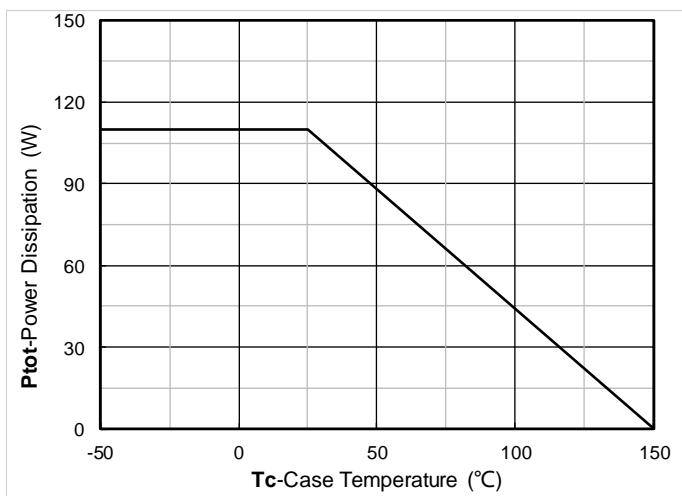


Figure 12. Power dissipation



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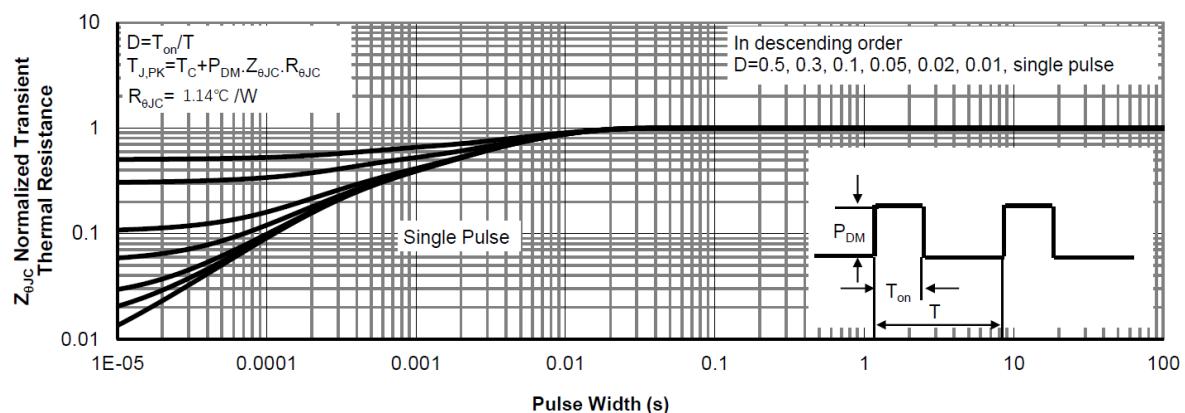
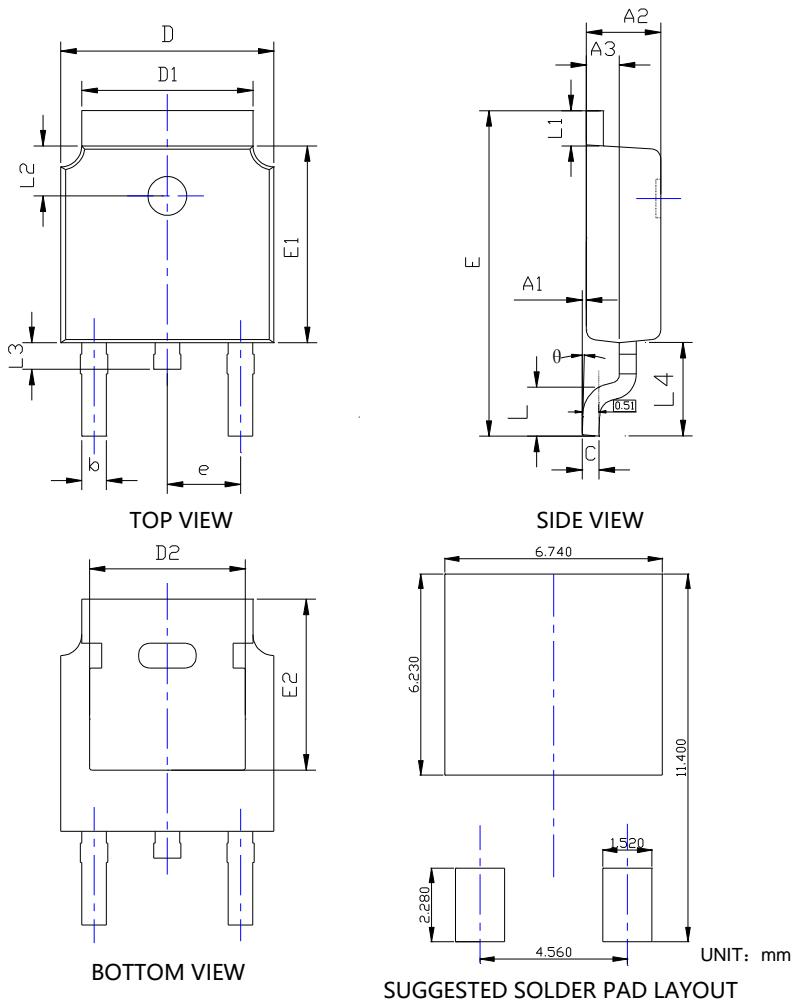


Figure13. Normalized Maximum Transient Thermal Impedance



■ TO-252-B Package information



SYMBOL	DIMENSIONS			Millimeter		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A1	0.000	---	0.008	0.000	---	0.200
A2	0.087	0.091	0.094	2.200	2.300	2.400
A3	0.035	0.039	0.043	0.900	1.000	1.100
b	0.026	0.030	0.034	0.660	0.760	0.860
c	0.018	0.020	0.023	0.460	0.520	0.580
D	0.256	0.260	0.264	6.500	6.600	6.700
D1	0.203	0.209	0.215	5.150	5.300	5.450
D2	0.181	0.189	0.195	4.600	4.800	4.950
E	0.390	0.398	0.406	9.900	10.100	10.300
E1	0.236	0.240	0.244	6.000	6.100	6.200
E2	0.203	0.209	0.215	5.150	5.300	5.450
e	0.090BSC			2.286BSC		
L	0.049	0.059	0.069	1.250	1.500	1.750
L1	0.035	---	0.050	0.900	---	1.270
L2	0.055	---	0.075	1.400	---	1.900
L3	0.240	0.310	0.039	0.600	0.800	1.000
L4	0.114REF			2.900REF		
theta	0°	---	10°	0°	---	10°

NOTE:

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



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