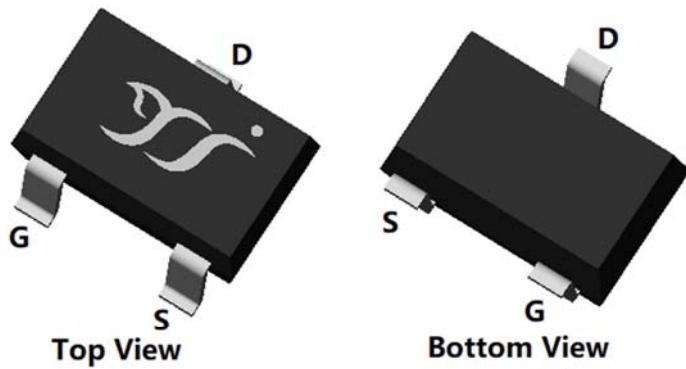
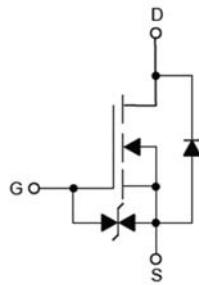


N-Channel Enhancement Mode Field Effect Transistor

**SOT-323**

Product Summary

- V_{DS} 60V
- I_D 300mA
- $R_{DS(ON)}$ (at $V_{GS}=10V$) $<2.0\text{ohm}$
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) $<2.5\text{ohm}$
- ESD protected up to 2.0kV (HBM)

General Description

- Trench Power MV MOSFET technology
- Voltage controlled small signal switch
- Low input Capacitance
- Fast Switching Speed
- Low Input / Output Leakage
- Part no. with suffix "Q" means AEC-Q101 qualified

Applications

- Battery operated systems
- Solid-state relays
- Direct logic-level interface: TTL/CMOS
- 12V, 24V Automotive systems

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

| Parameter | Symbol | Limit | Unit |
|--|-----------------|----------|-----------------------------|
| Drain-source Voltage | V_{DS} | 60 | V |
| Gate-source Voltage | V_{GS} | ± 20 | V |
| Drain Current @ $T_A=25^\circ\text{C}$ | I_D | 300 | mA |
| Pulsed Drain Current ^A | I_{DM} | 1.5 | A |
| Total Power Dissipation @ $T_A=25^\circ\text{C}$ | P_D | 416 | mW |
| Thermal Resistance Junction-to-Ambient @ Steady State ^B | $R_{\theta JA}$ | 360 | $^\circ\text{C} / \text{W}$ |
| Junction and Storage Temperature Range | T_J, T_{STG} | -55~+175 | $^\circ\text{C}$ |

■ Ordering Information (Example)

| PREFERRED P/N | PACKING CODE | Marking | MINIMUM PACKAGE(pcs) | INNER BOX QUANTITY(pcs) | OUTER CARTON QUANTITY(pcs) | DELIVERY MODE |
|---------------|--------------|---------|----------------------|-------------------------|----------------------------|---------------|
| 2N7002KDWHQ | F2 | 72KD. | 3000 | 30000 | 120000 | 7" reel |



2N7002KDHQ

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|-----------------------------------|---------------------|--|-----|------|-----|-------|
| Static Parameter | | | | | | |
| Drain-Source Breakdown Voltage | BV _{DSS} | V _{GS} = 0V, I _D =250μA | 60 | | | V |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{DS} =60V, V _{GS} =0V | | | 1 | μA |
| Gate-Body Leakage Current | I _{GSS} | V _{GS} = ±20V, V _{DS} =0V | | | ±10 | μA |
| Gate Threshold Voltage | V _{GS(th)} | V _{DS} = V _{GS} , I _D =250μA | 1.1 | 1.5 | 2.4 | V |
| Static Drain-Source On-Resistance | R _{DS(ON)} | V _{GS} = 10V, I _D =300mA | | 1.1 | 2.0 | Ω |
| | | V _{GS} = 4.5V, I _D =200mA | | 1.3 | 2.5 | |
| Diode Forward Voltage | V _{SD} | I _S =115mA, V _{GS} =0V | | 0.9 | 1.2 | V |
| Gate resistance | R _G | f=1MHz | | 150 | | Ω |
| Dynamic Parameters | | | | | | |
| Input Capacitance | C _{iss} | V _{DS} =25V, V _{GS} =0V, f=1MHZ | | 25 | | pF |
| Output Capacitance | C _{oss} | | | 8 | | |
| Reverse Transfer Capacitance | C _{rss} | | | 4 | | |
| Switching Parameters | | | | | | |
| Total Gate Charge | Q _g | V _{GS} =10V, V _{DS} =30V, I _D =1A | | 1.75 | | nC |
| Gate Source Charge | Q _{gs} | | | 1.00 | | |
| Gate Drain Charge | Q _{gd} | | | 0.25 | | |
| Reverse Recovery Charge | Q _{rr} | I _{SD} =1A, di/dt=100A/us | | 3.9 | | nC |
| Reverse Recovery Time | t _{rr} | | | 15 | | ns |
| Turn-on Delay Time | t _{D(on)} | V _{GS} =10V, V _{DS} =30V, I _D =1A, R _g =3Ω | | 4.6 | | ns |
| Turn-on Rise Time | t _r | | | 20.0 | | |
| Turn-off Delay Time | t _{D(off)} | | | 10.5 | | |
| Turn-off Fall Time | t _f | | | 25.5 | | |

A. Repetitive rating; pulse width limited by max. junction temperature.

B. The value of R_{θJA} is measured with the device mounted on the minimum recommend pad size, in the still air environment with T_A =25°C. The maximum allowed junction temperature of 175°C. The value in any given application depends on the user's specific board design.



2N7002KDWHQ

■ Typical Performance Characteristics

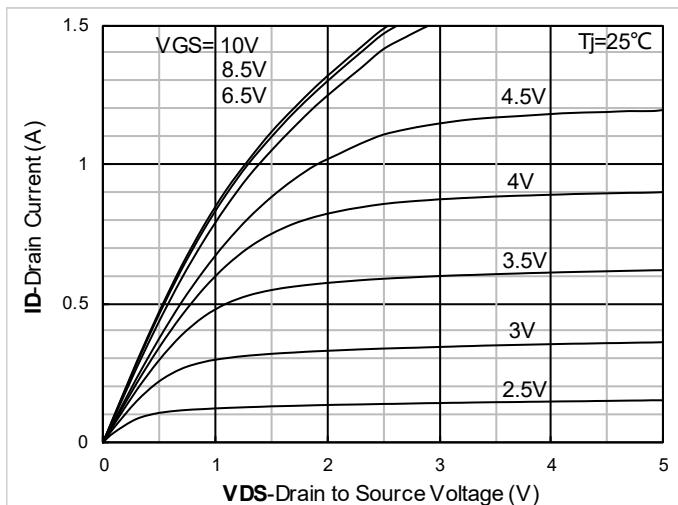


Figure1. Output Characteristics

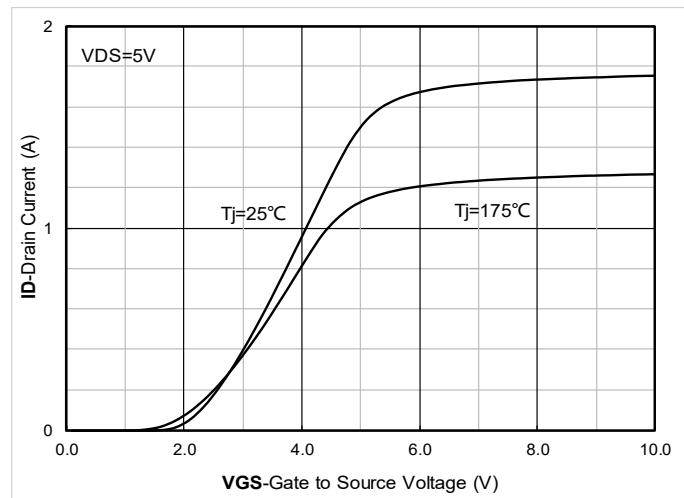


Figure2. Transfer Characteristics

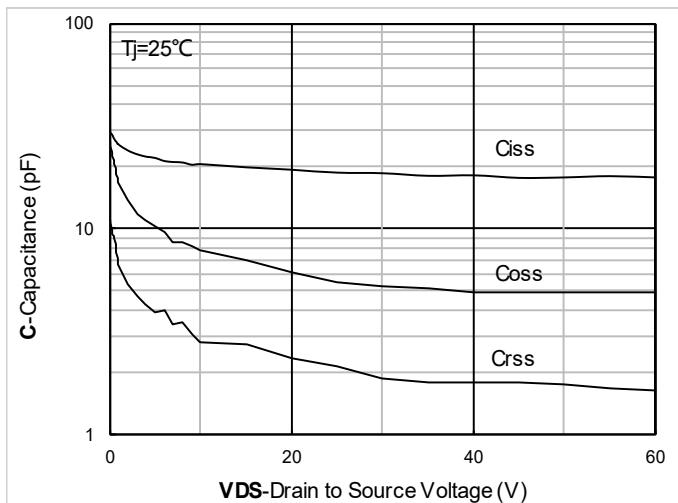


Figure3. Capacitance Characteristics

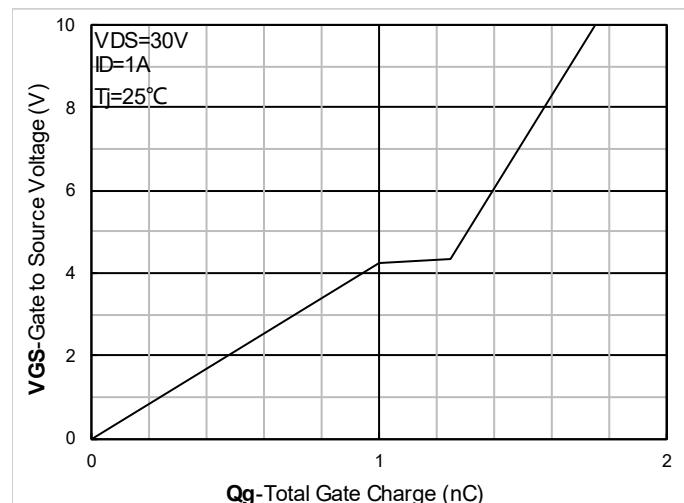


Figure4. Gate Charge

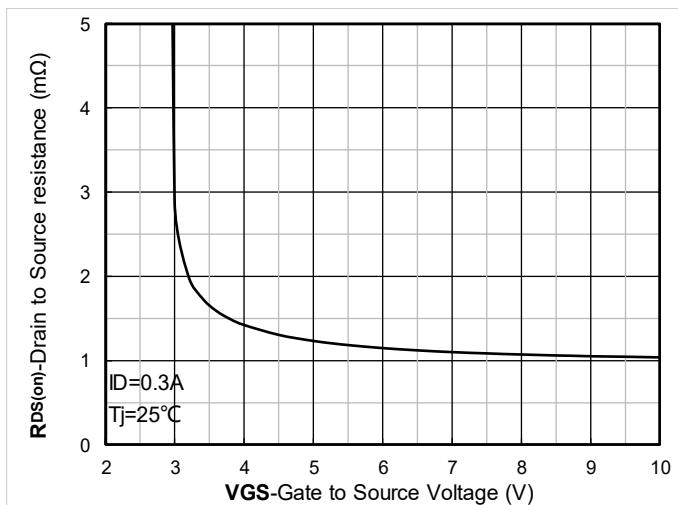


Figure5. On-Resistance vs Gate to Source Voltage

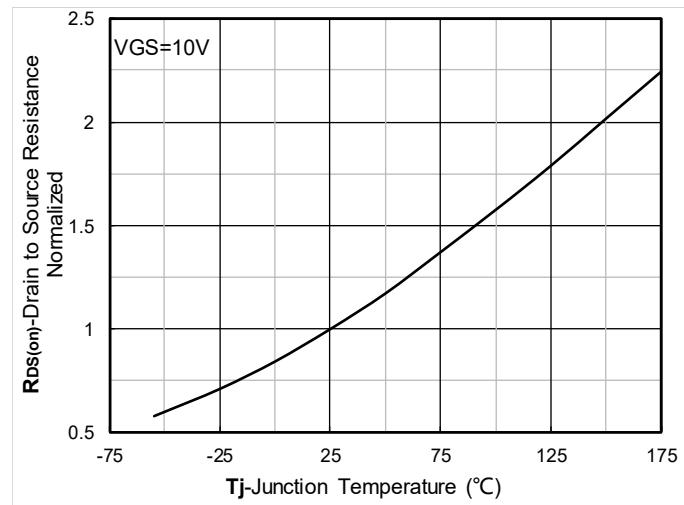


Figure6. Normalized On-Resistance



2N7002KDWHQ

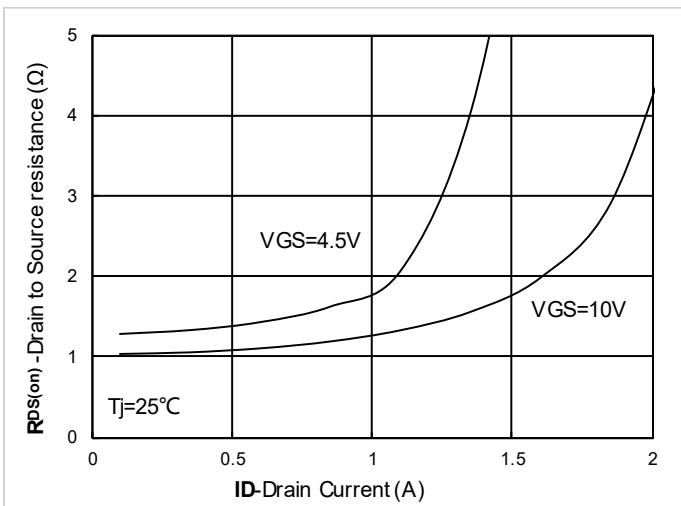


Figure 7. $R_{DS(on)}$ VS Drain Current

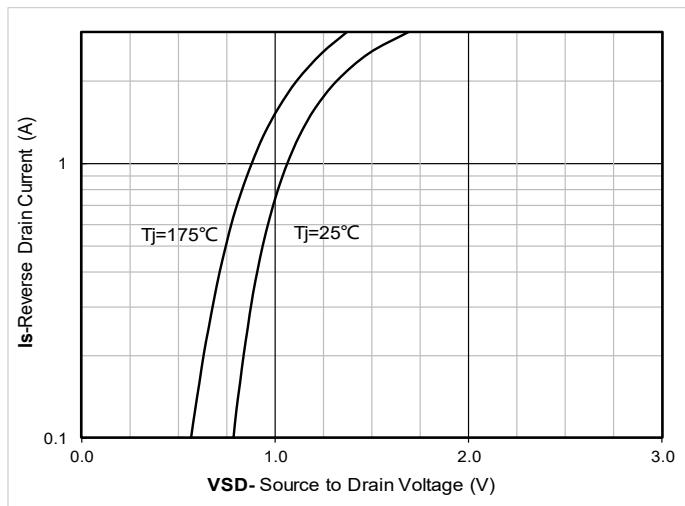


Figure 8. Forward characteristics of reverse diode

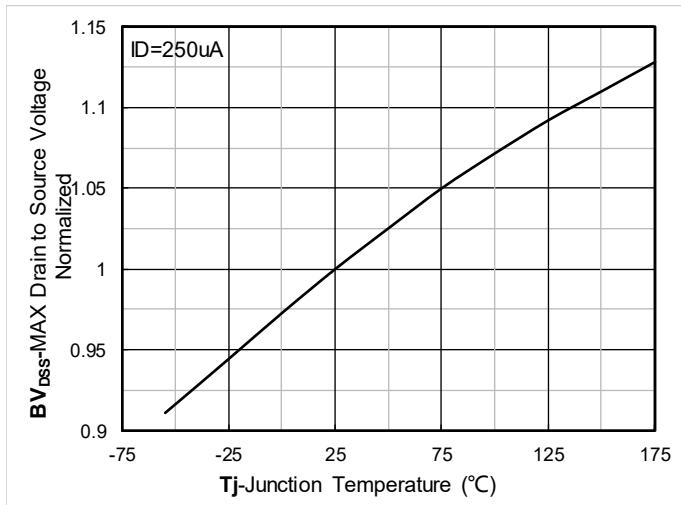


Figure 9. Normalized breakdown voltage

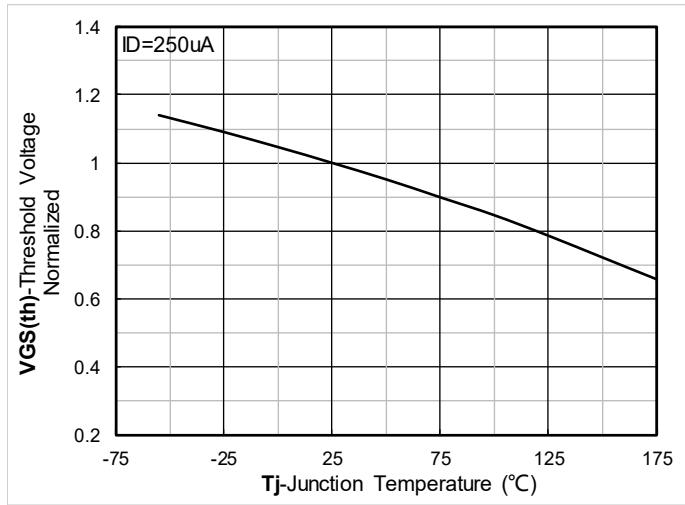


Figure 10. Normalized Threshold voltage

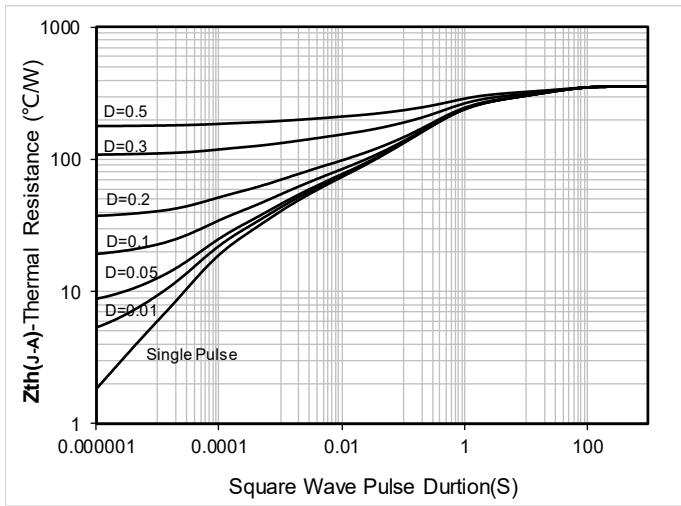


Figure 11. Maximum Transient Thermal Impedance

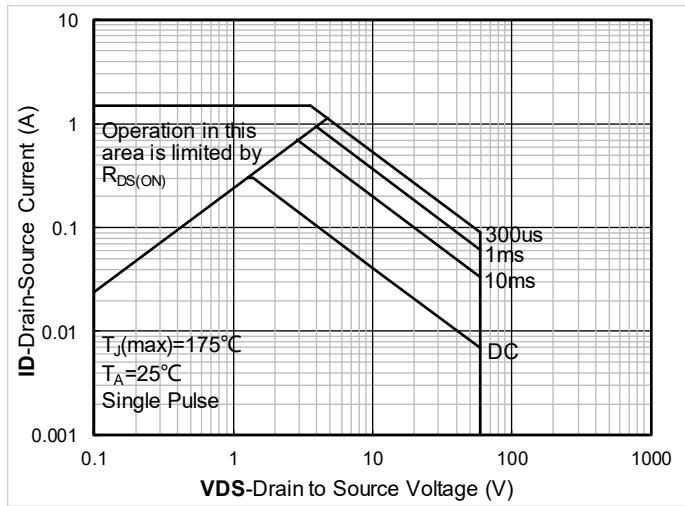


Figure 12. Safe Operation Area

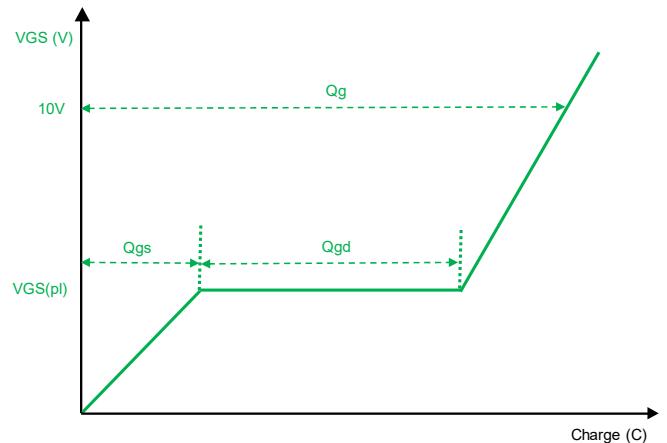
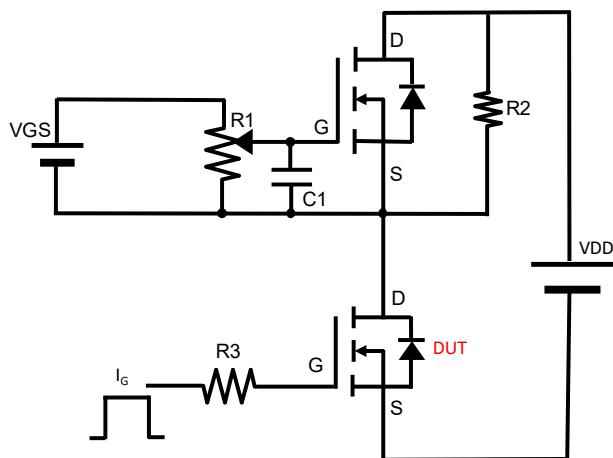
**■ Test Circuits & Waveforms**

Figure A. Gate Charge Test Circuit & Waveform

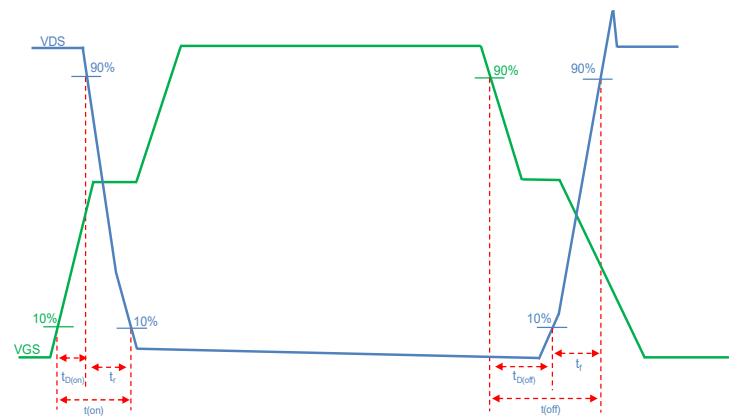
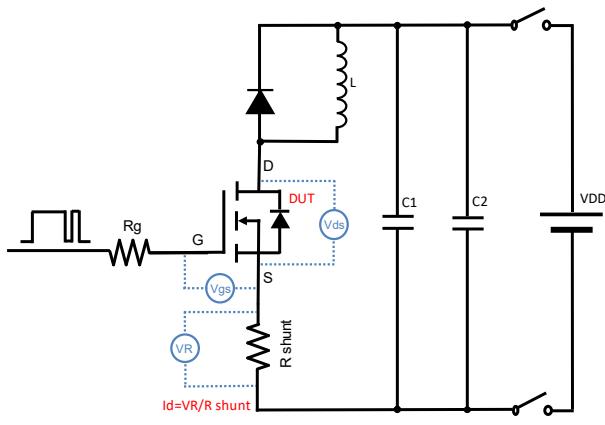


Figure B. Resistive Switching Test Circuit & Waveform

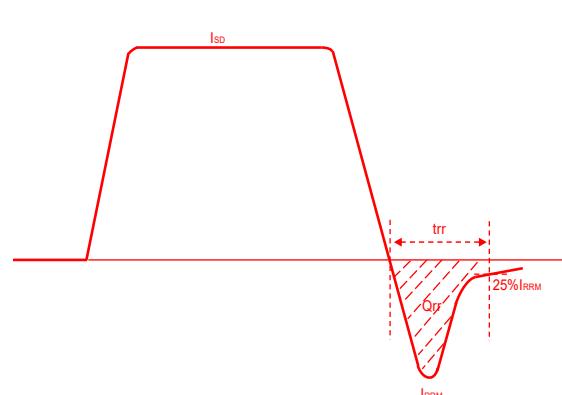
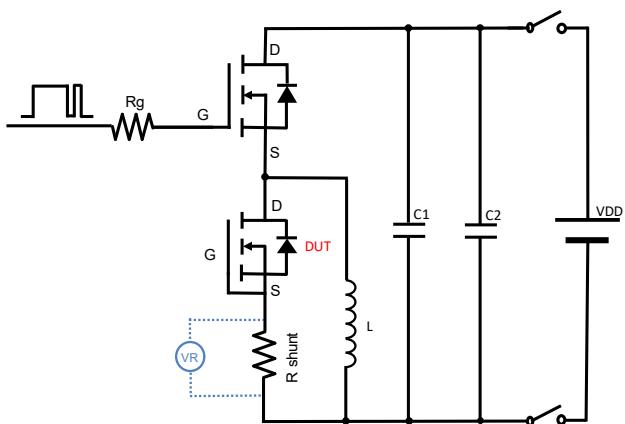
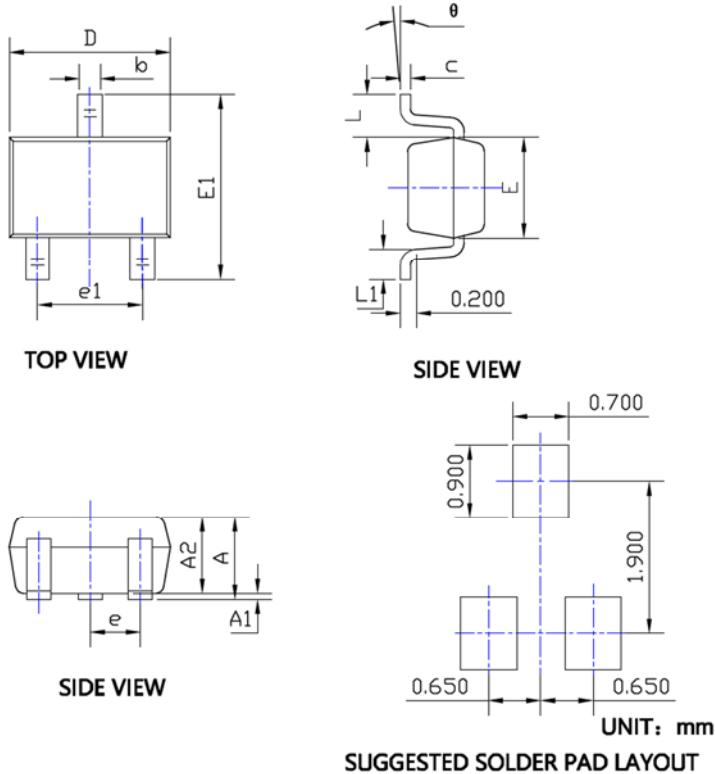


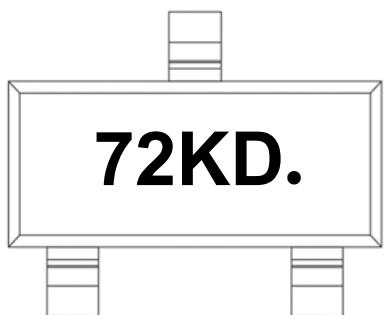
Figure C. Diode Recovery Test Circuit & Waveform

**■ SOT-323 Package Outline Dimensions**

| SYMBOL | DIMENSIONS | | | |
|--------|------------|------------|-------|-------|
| | INCHES | Millimeter | MIN. | MAX. |
| A | 0.035 | 0.043 | 0.900 | 1.100 |
| A1 | 0.000 | 0.004 | 0.000 | 0.100 |
| A2 | 0.035 | 0.039 | 0.900 | 1.000 |
| b | 0.006 | 0.016 | 0.150 | 0.400 |
| c | 0.004 | 0.010 | 0.100 | 0.250 |
| D | 0.071 | 0.087 | 1.800 | 2.200 |
| E | 0.045 | 0.053 | 1.150 | 1.350 |
| E1 | 0.085 | 0.096 | 2.150 | 2.450 |
| e | 0.026TYP | 0.650TYP | | |
| e1 | 0.047 | 0.055 | 1.200 | 1.400 |
| L | 0.021REF | 0.525REF | | |
| L1 | 0.010 | 0.018 | 0.260 | 0.460 |
| θ | 0° | 8° | 0° | 8° |

NOTE:

- 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

■ Marking Information**Note:**

1. All marking is at middle of the product body
2. All marking is in laser marking
3. 72KD is Marking Code
4. Body color: Black



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